Analysing and Modeling the Implicated Noise in the Front-End of ACORDE using a Mixed-Mode design method: FPAA-FPGA Architecture

Carlos Graciós, German Ardul Munoz-Hernandez, Héctor, Alejandro Diaz-Sanchez, Jorge Hermelindo Barrera

Abstract—Novel mixed-model architecture can be used to design and apply Instrumental solutions to reduce the new problems to be address in the actual fault tolerance requirement for the High Energy Physics experiments as the TLEP proposition. This article is a first approach of the novel Fault Tolerance Field-Programmable Mixed mode architectures to be applied in the Instrumentation and control schemes for the new TLEP Experiment. Due to the Mixed mode architectures include both the digital and the analogue techniques, several advantage but practical restrictions have been determined in this report. Because of the new requirements which must be accomplished, the analysis of these new implications is described.

I. INTRODUCTION

New and interesting results have been reported in the High Energy Physics Experiments. Hence the most relevant goal has been the verification of the Higgs Boson center of mass next to the other level of energy presented at 350 GeV [1].

It is well-known that the technical level for the design on new detectors have raised the question of what new technical implications must be design and apply in the novel experiment and how it should be acquired. It would be a challenge to apply the recent strategies and techniques to resolve electrical and magnetic compromises in the Instrumental and Control of each subsystem in the next Circular Collider.

Then to extend the results of [2] including the improvement in the Front - End design reported in [3], the methodology described by Graciós is proposed [4].

It is well known that the new electronic architectures can apply analogue and digital System on a Chip but there are not several real improvements applied in Recent Circular Collider. The groundbreaking work of Graciós et al [4] on the modeling and control of Programable structures has found attention by the industrial community as a major advance. On the other hand, it is essential to consider that the use of the FP mixed strategies in the Instrumentation and control of High Energy Physics may be a great opportunity to develop and reach new challenges with the benefits of both design prototyping.

II. FUNDAMENTAL CONCEPTS

It is well-known that the novel High Energy Physics Experiments (HEPE) represents a great challenge in terms of

Carlos Graciós is with CERN
German Ardul Munoz-Hernandez is with Affiliation not available
Héctor is with Affiliation not available
Alejandro Diaz-Sanchez is with Affiliation not available
Jorge Hermelindo Barrera is with Affiliation not available

the Design for Structural and Functional parametrical detector behavior on Future Circular Collider (FCC). One of this particular aims is the low voltage power distribution to the front-end electronics embedded in this type of architectures [5].

Several constraints must to be considered and resolve taking into account the preliminary design for the whole instrumental and control schemes. The internal current from detectors must be more efficient in the distribution process for voltage regulation, power transmission lines and signal processing and filtering.

Accord with the evolution in IC technology, the design of this type of architectures can be improvement applying the nano-metric scales of integration between 130 to 65 nm CMOS by low-voltage low-power technique design.

It is needed to obtain new adaptive software-hardware schemes to reach the new measurement parameters to support high magnetic fields where the inductor structure beacuse it is not adequate for the magnetic core fully saturated [6]. The extremely high radiation levels within hadron collider (e.g. LHC and HLLHC) experiments will cause commercial devices to fail "immediately", either because of total dose or because of radiation induced single event effects (e.g. single event burnout). Only dedicated and highly optimized power conversion components can survive in such an environment.

The active power conversion integrated circuits will have to stand relatively high voltages (10 V), but semiconductor technologies working at that voltage level, are unfortunately known to be particular sensitive to radiation effects. Hence, significant dedicated HV IC technology radiation qualification work combined with detailed and specialized circuit and IC layout work is required to implement reliable data processing structures.

Several experimental front-end ASICs with built in shunt regulators have been successfully designed in the community and small-scale system tests have shown encouraging results [7].

These type of required ASICs can be design to process the signals associated at the Instrumentation and Control schemes for the Front-End devices inserted in the detectors for FCC.

However, only, digital or analogue architectures can be found in recent detector but a mixed-mode strategy is quite new.

Finally for future experiments which aim to work with pulsed beams (e.g. ILC, CLIC, FCC), where the detectors only need to be sensitive for a fraction of the time, the

use of adaptive and mixed-mode signal processing data is a very attractive option for minimizing the implicated noise and reduced the dissipated power inside the detector with Fast Computational Architectures (FCA).

Maintaining stable and low noise performance of the analogue parts of millions of multiple channels is a major challenge requiring significant R&D activities for both the front-end ASIC's and the global parameters distribution system in FCC and its components [8].

The architecture of the global power distribution system, the implementation and use of local power conversion techniques (on-module and/or on-chip) will have a major impact on the actual physics performance of many detectors (FCC). There must be a well-organized and continuous R&D effort in the HEP community as each new experiment (or upgrade) poses new challenges (higher radiation levels, decreasing power supply voltage for front-end chips, increasing constraints on material budget and cooling, pulsed power optimized for a particular experiments, etc.).

III. ADAPTIVE FILTERING

According to Belloni [9] there exist several new requirements for the electronic applications. (See fig .1) These new requirements can be more exigent in terms of the level of applications schemes. This is the particular challenge area of High Physic Energy Instrumentation.

Recently, several improvements in Physics Instrumental have been developed, tested and applied considering some particular issues such as: Bandwidth (BW), Noise (S/R) and Low Voltage/Low Power (LV/LP) characteristics. Nevertheless, some authors have reported the possibility to improve in other performance index of the dynamic measurements.

Some of this type of architecture have been designed, described and integrated considering one of the two design method; i, e, Analogue or Digital. However, if one of them is used for the whole integration system then it is possible to reduce the performance in other parameters.

In terms of Adaptive Filtering, several contributions have been made. Accord to [10] several type of algorithms are reported to achieve the new filter requirement. One of this type of parameters is the noise implication in design.

By this asseveration, it is desirable to obtained a more robust architecture which can accomplish the accurate level of parametric indexes for the complete design [11].

Obviously, these parameters must be measured with the adequate sensors to match in the design structure [12].

A way to improve the sensor measurements is by using smart-sensors which commonly perform self-adjusting, signal filtering, transducer resolution increasing, and fused parameters estimating functions. Furthermore, smart sensors are utilized to measure variables such as temperature, voltage and current, motion dynamics, kinematics, and many other derived variables such as Luminosity, and other physical variables [13].

Let Ch_1(t) be the ACORDE Front-End Output signal, which can be divided in the addition of the s_1(t) and its implicated noise n_1(t), defined by:

$$Ch_1 = s_1(t) + n_1(t). \tag{1}$$

And let Ch_2(t) for the processing channel in the output FPAA:

$$Ch_2(t) = s_2(t) + n_2(t)$$

Now, for any signal with delay:

$$y(t) = x(t - t_d) + n(t)$$

where t_d = delay time and $x(t)$ is the original signal and $y(t)$ is the signal with delay and noise signal then, the Cross Correlation can be defined by:

$$R_{yx}(\tau) = \lim_{T \to \infty} \int_{-T/2}^{T/2} y(t + \tau) x^*(t) dt))$$

Considering $Ch_1(t) = x(t)$ and $Ch_2(t) = y(t)$ then the last expression is rewritten as:

$$R_{Ch_2(t)Ch_1(t)}(\tau) = \lim_{T \to \infty} \int_{-T/2}^{T/2} Ch_2(t + \tau) Ch_1(t) dt$$

Expanding for the delay time...

$$R_{Ch_2(t)Ch_1(t)}(\tau) = \lim_{T \to \infty} \frac{1}{T} \int_{-T/2}^{T/2} [Ch_1(t - t_d + \tau) + n(t + \tau)] Ch_1^*(t) dt$$

It implies:

$$R_{Ch_1(t)Ch_1(t)}(\tau) = R_{Ch_1Ch_1}(\tau - t_d) + R_{nCh_1(t)}(\tau)$$

If in any testing procedure with white noise added at the experimental approaching:

$$R_{uu}(\tau) = \frac{1}{2}$$

then the Autocorrelation is a constant value equal to 1/2, it is the spectral density of power is its Fourier transform itself. By this assumption, the autocorrelation by white noise definition can be used to evaluate the relationship between the two signals correlated by noise influence.

IV. MIXED- MODE ARCHITECTURE PROPOSED

Mixed mode architecture proposed [14] is based on FPGA Altera Max II Development Kit which is embedded a dynamic PIC structure by FPAA prototyping board (See Fig. 2). The FPGA is used to describe the structure and function of the PIC in the FPAA board to modify the Switched Capacitor Frequency in closed-loop scheme. This whole architecture will function as an adaptive filter to reduce the noise in the ACORDE signal processing.

It is possible because the FPAA architecture processes the signal in analogue form and the digital conversion develop by the FPGA scheme is not required.

Nevertheless, figure 4 shows the strategy used to obtain the improved design with the hybrid architecture. The equation described by the Anadigm designer group was determined to generate the frequency response for the FPGA in terms of the changes in the noise signal.

The adjust loop is realized by the disability of the PIC in the FPAA Borad and the signals paths for the FPGA Development Board as well.
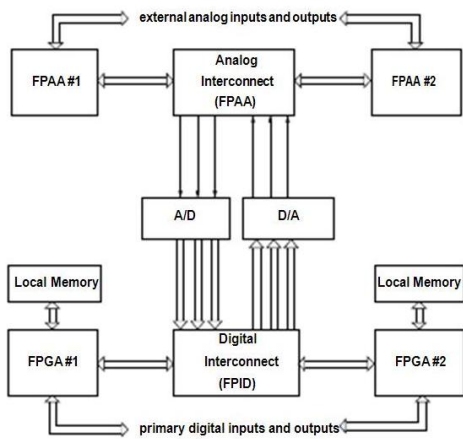
Figure 1.   FPAA - PFGA Architecture proposed See fig. 3 to review the FPGA Deveploment Board applied in this experiment...
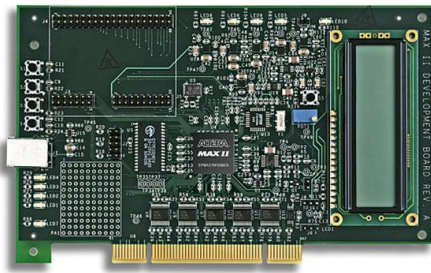

Figure 2.   Altera Max II Development Board In this board, a EPM1270 FPGA is described the PIC used in the FPAA prototyping board to adapt the frequency response for the Front-End scheme.

Scheduling the firing signals for each SC sub-circuit the adaptive algorithm is obtained.

Nevertheless, figure 4 shows the strategy used to obtain the improved design with the hybrid architecture. The equation described by the Anadigm designer group was determined to generate the frequency response for the FPGA in terms of the changes in the noise signal.

The adjust loop is realized by the disability of the PIC in the FPAA Borad and the signals paths for the FPGA Development Board as well.
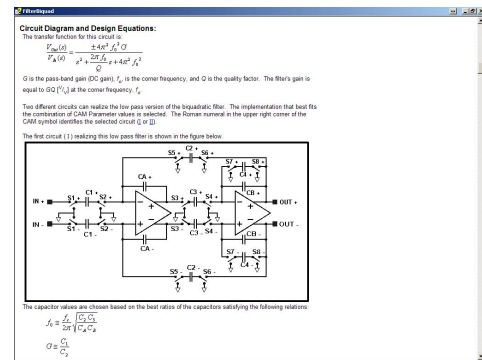
Scheduling the firing signals for each SC sub-circuit the adaptive algorithm is obtained.

Figure 5 is showed to describe the form to pre-programming the internal architecture of the adaptive filter.

Then Figure 6 and 7 show the Bode and Z-states for the first approach and obtaining the primary result for the Front -End in figure 8.

Figure 8 let to compare the simulation result of the actual filter installed in the Front-End of ACORDE-ALICE architecture. The simulator is Modelsim for Quartus II Web Edition. Note the Noise correlated at the signal with at reduction obtained of 10

In this case, Channel 1 is the original Front-End signal and Channel 2 shows the output for the adaptive filter. The noise reduction is about 5% with the architecture proposed.
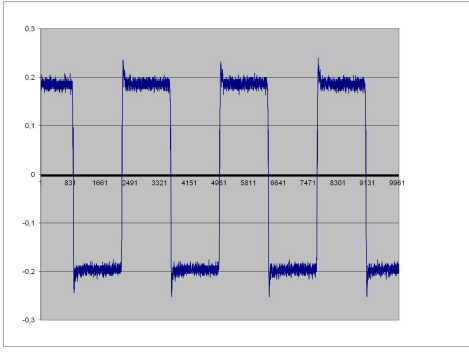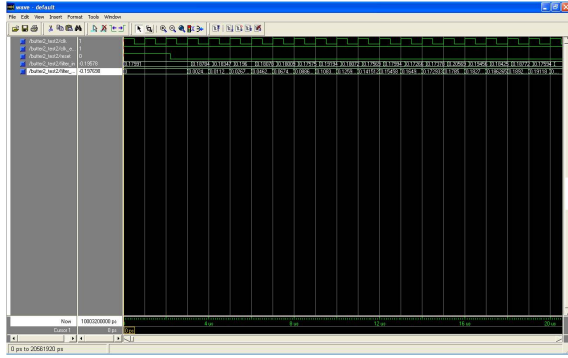

Figure 3.   Design scheme based on FPAA Architecture.

Figure 4.   Design platform for FPAA Architecture

Figure 5.   Frequency response

Figure 6.   Results using FPAA architecture

Figure 7. Original ACORDE Front-End signal

Figure 8. Pulses on Single FPGA architecture

Figure 9. Signal result with new architecture

Figure 10. Replace this text with your caption

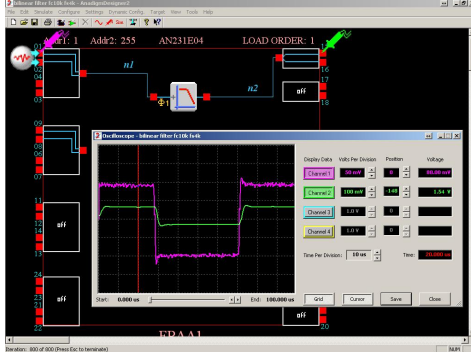Figure 11. White noise comparing

V. RESULTS

We begin by considering a simple special case. Obviously, every simply simulation demonstrate the possibility to improve the noise reduction in the signal. Clearly, if the design provide the advantages for the mixed-design then some requirements must be satisfy. Because the Clock signal for the FPAA is adjusted at the noise-event, if the change is intermittent to the velocity response for the device then is undesirable, non-suitable and with unstable behavior. Therefore if the architecture is stable then it will be applies for a specific ranges of signal values for event.
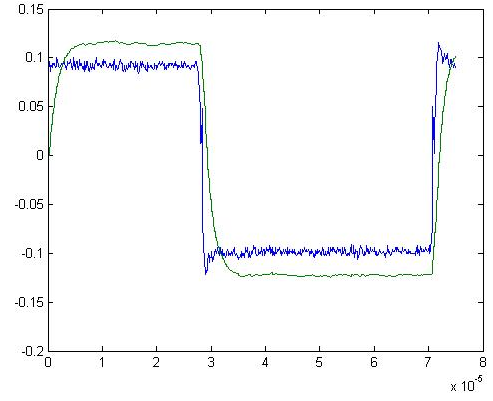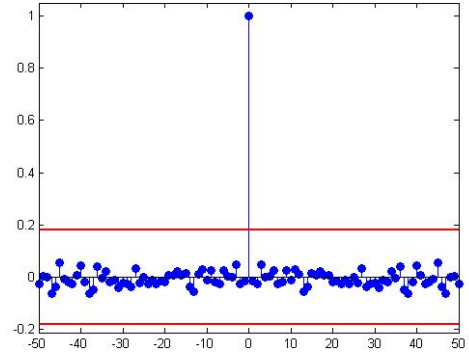
A. Residual Analysis with Autocorrelation.

In this part a statistical analysis shows how to use autocorrelation with a confidence interval to analyze the residuals of a least-squares fit to noisy data in both two signal i.e. the original front-end filter design (Ch1) and the improved signal measured at the output of the FPGAA adaptive architecture Ch2. Then the residuals are the differences between the fitted model (Ch1) and the data (Ch2).

Considering the theory proposed in a signal-plus-white noise model, if a good fit for the signal is proposed, the residuals should be white noise.

The additive noise is a sequence of uncorrelated random variables following a N(0,1) distribution. This means that all the random variables have mean zero and unit variance. Set the random number generator to the default settings for reproducible results.

The analysis was export at classical algorithm developed for Matlab because it is an adequate platform for signal analysis considering the toolboc added in its environment.

Using the polyfit command to find the least-squares line for the noisy data it is possible to plot the original data along with the least-squares fit showed in figure .

Findind the residuals, it is necessary to obtain the autocorrelation sequence of the residuals to lag 50.When you inspect the autocorrelation sequence, you want to determine whether or not there is evidence of autocorrelation. In other words, you want to determine whether the sample autocorrelation sequence looks like the autocorrelation sequence of white noise. If the autocorrelation sequence of the residuals looks like the autocorrelation of a white noise process, you

are confident that none of the signal has escaped your fit and ended up in the residuals. In this analysis, a 99%confidence interval is applied. To construct the confidence interval to know the distribution of the sample autocorrelation values is needed. But also to find the critical values on the appropriate distribution between which lie 0.99 of the probability is defined.

Because the distribution in this case is Gaussian, a complementary inverse error function is required. The matlab command is defined as erfcinv. The relationship between this function and the inverse of the Gaussian cumulative distribution function is described on Matlab Help Page.

In figure NN, the complete algorithm is described. The principal steps can be resumed as follows:

1) Fitting the data. 2) Defining the experiment for White noise. 3) Finding the critical value for the 99% confidence interval. 4) Using the critical value to construct the lower and upper confidence bounds. 5) Plotting the autocorrelation sequence along with the 99%confidence intervals.

Except at zero lag, the sample autocorrelation values lie within the 99%confidence bounds for the autocorrelation of a white noise sequence. At this part of the analysis, it can conclude that the residuals are white noise. More specifically, it cannot reject that the residuals are a realization of a white noise process for both signals.

Now, considering that the data are sampled at 100 kHz then the frequency of the experiment can be set for the random number generator to the default settings for reproducible results.

Using the discrete Fourier transform (DFT) to obtain the least-squares, then, the random signal is fitting to both channels 100 kHz. The least-squares estimate of the amplitude is 2 / N times the DFT coefficient corresponding to 100 kHz, where N is the length of the signal. In this part, DFT bin 101 corresponds to 100 kHz.Find the residuals and determine the sample autocorrelation sequence to lag 50.

Therefore, plotting the autocorrelation sequence with the 99% confidence intervals. Again, except at zero lag, the sample autocorrelation values lie within the 99% confidence bounds for the autocorrelation of a white noise sequence.

From this, it is concluded that the residuals are "white noise". More specifically, it is not possible to reject that the residuals are a realization of a white noise process.

Finally, add another sine wave with a frequency of 200 Hz and an amplitude of 3/4. Fit only the sine wave at 100 Hz and find the sample autocorrelation of the residuals.

In this case, the autocorrelation values clearly exceed the 99%confidence bounds for a white noise autocorrelation at many lags. Here you can reject the hypothesis that the residuals are a white noise sequence. The implication is that the model has not accounted for all the signal and therefore the residuals consist of signal plus noise.

VI. Conclusions

This work shows the analysis and modeling with a new mixed-mode architecture based and FPAA-FPGA architecture...

References

[1] Bundel, "LEP3: A High Luminosity e+e- Collider to Study the Higgs Boson," *arXiv:1208.0504, submission 138 to ESPP 2012*, vol. 0, p. 0, aug 2012.

[2] A. F. Tellez, "The ALICE experiment at the CERN - LHC," *Jinst*, vol. 1, pp. 1–260, sep 2009.

[3] G. A. Muñoz-Hernandez, "Implication of Electric Noise in the ACORDE Front-End Electronics of the ALICE Experiment," *IEEE Digital Library:10.1109/CONIELECOMP.2008.9*, vol. 1, pp. 148–153, mar 2008.
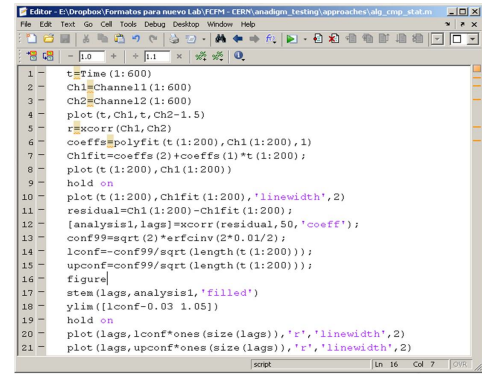
Figure 12. Matlab Algorithm

[4] C. A. Gracios-Marin, *Fuzzy Scheduling Applied on Hydroelectric Power Generation.* Intech, 2012.

[5] F. Anghinolfi, P. Aspell, M. Campbell, E. Heijne, P. Jarron, and G. Meddeler, "Development of Front End Electronics for Future Supercollider Experiments," in *New Technologies for Supercolliders.* Springer US, 1991, pp. 105–123. [Online]. Available: http://dx.doi.org/10.1007/978-1-4684-1360-1_9

[6] E. G. Ramirez, I. Garcia, E. Guerrero, and C. Pacheco, "A tool for supporting the design of DC-DC converters through FPGA-based experiments," *IEEE Latin America Transactions*, vol. 14, no. 1, pp. 289–296, jan 2016. [Online]. Available: http://dx.doi.org/10.1109/TLA.2016.7430091

[7] E. Cabal-Yepez, A. G. Garcia-Ramirez, R. J. Romero-Troncoso, A. Garcia-Perez, and R. A. Osornio-Rios, "Reconfigurable Monitoring System for Time-Frequency Analysis on Industrial Equipment Through STFT and DWT," *IEEE Transactions on Industrial Informatics*, vol. 9, no. 2, pp. 760–771, may 2013. [Online]. Available: http://dx.doi.org/10.1109/TII.2012.2221131

[8] M. Bicer, H. D. Yildiz, I. Yildiz, G. Coignet, M. Delmastro, T. Alexopoulos, C. Grojean, S. Antusch, T. Sen, H.-J. He, K. Potamianos, S. Haug, A. Moreno, A. Heister, V. Sanz, G. Gomez-Ceballos, M. Klute, M. Zanetti, L.-T. Wang, M. Dam, C. Boehm, N. Glover, F. Krauss, A. Lenz, M. Syphers, C. Leonidopoulos, V. Ciulli, P. Lenzi, G. Sguazzoni, M. Antonelli, M. Boscolo, U. Dosselli, O. Frasciello, C. Milardi, G. Venanzoni, M. Zobov, J. van der Bij, M. de Gruttola, D.-W. Kim, M. Bachtis, A. Butterworth, C. Bernet, C. Botta, F. Carminati, A. David, L. Deniau, D. d'Enterria, G. Ganis, B. Goddard, G. Giudice, P. Janot, J. M. Jowett, C. Lourenço, L. Malgeri, E. Meschi, F. Moortgat, P. Musella, J. A. Osborne, L. Perrozzi, M. Pierini, L. Rinolfi, A. de Roeck, J. Rojo, G. Roy, A. Sciabà, A. Valassi, C. S. Waaijer, J. Wenninger, H. Woehri, F. Zimmermann, A. Blondel, M. Koratzinos, P. Mermod, Y. Onel, R. Talman, E. C. Miranda, E. Bulyak, D. Porsuk, D. Kovalskyi, S. Padhi, P. Faccioli, J. R. Ellis, M. Campanelli, Y. Bai, M. Chamizo, R. B. Appleby, H. Owen, H. M. Cuna, C. Gracios, G. A. Munoz-Hernandez, L. Trentadue, E. Torrente-Lujan, S. Wang, D. Bertsche, A. Gramolin, V. Telnov, M. Kado, P. Petroff, P. Azzi, O. Nicrosini, F. Piccinini, G. Montagna, F. Kapusta, S. Laplace, W. da Silva, N. Gizani, N. Craig, T. Han, C. Luci, B. Mele, L. Silvestrini, M. Ciuchini, R. Cakir, R. Aleksan, F. Couderc, S. Ganjour, E. Lançon, E. Locci, P. Schwemling, M. Spiro, C. Tanguy, J. Zinn-Justin, S. Moretti, M. Kikuchi, H. Koiso, K. Ohmi, K. Oide, G. Pauletta, R. R. de Austri, M. Gouzevitch, and S. Chattopadhyay, "First look at the physics case of TLEP," *Journal of High Energy Physics*, vol. 2014, no. 1, jan 2014. [Online]. Available: http://dx.doi.org/10.1007/JHEP01(2014)164

[9] M. Belloni and F. Maloberti, "DC-DC Converters Low-Noise Amplifier for portable applicatios," *Doctoral Thesis Di Ricerca*, vol. 1, pp. 1–155, dec 2010.

[10] M. E. Iglesias, "Implementation of QRD-RLS algorithm on FPGA. Application to Noise Canceller System," *IEEE Latin America Transactions*, vol. 9, no. 4, pp. 458–462, jul 2011. [Online]. Available: http://dx.doi.org/10.1109/TLA.2011.5993728

[11] R. Castaneda-Sheissa, A. Sarmiento-Reyes, L. Hernandez-Martinez, and H. Vazquez-Leal, "A CAD tool for automated bandwidth design of negative feedback amplifiers," in *48th Midwest Symposium on Circuits and Systems 2005*. Institute of Electrical & Electronics Engineers (IEEE), 2005. [Online]. Available: http://dx.doi.org/10.1109/MWSCAS.2005.1594250

[12] A. J. Rojas, "Signal-to-Noise Ratio Limitations in Feedback Control," *IEEE Latin America Transactions*, vol. 9, no. 5, pp. 690–699, sep 2011. [Online]. Available: http://dx.doi.org/10.1109/TLA.2011.6030977

[13] B. Muñoz-Barron, L. Morales-Velazquez, R. J. Romero-Troncoso, C. Rodriguez-Donate, M. Trejo-Hernandez, J. P. Benitez-Rangel, and R. A. Osornio-Rios, "FPGA-Based Multiprocessor System for Injection Molding Control," *Sensors*, vol. 12, no. 12, pp. 14 068–14 083, oct 2012. [Online]. Available: http://dx.doi.org/10.3390/s121014068

[14] C. Gracios-Marin, G. Munoz-Hernandez, A. Diaz-Sanchez, P. Nuno-de-la Parra, J. Estevez-Carreon, and C. Vega-Lebrúm, "Recursive decision-making feedback extension (RDFE) for fuzzy scheduling scheme applied on electrical power control generation," *International Journal of Electrical Power & Energy Systems*, vol. 31, no. 6, pp. 237–242, Jul 2009. [Online]. Available: http://dx.doi.org/10.1016/j.ijepes.2009.01.008