Synopsis of Current Consumption, PWM and DMA In Single Core, Dual Core and Multi Core Processors SoC

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***Abstract*—In this paper, the comparsion between pulse width modulation(PWM), Direct Memory Access(DMA), power supply and current consumption by peripherals and core in five processors viz., SAMD21G18A, TMS570LS0432, AM3352BZCED60, AM1808EZCE and XCZU3EG-1SBVA484E is studied from designing point of view in applications where power generation, power consumption and autonomy is critical. The contrast has been drawn from datasheets, reference manual and minor calculations and is basically a synopsis.**

***Index Terms*—AM1808EZWT3, AM3352BZCZA60, Sitara,Arm9, Cortex-A8, Multi Core, Dual Core, performance, TMS570LS04, Hercules, TMS570LS0432, SAMD21G18A, Zynq, UltraScale+, MPSoC, ZU3EG, SBVA484, lock-step, ARM®, Cortex®-R4, Cortex R5F, Cortex A53, SIMD, NEON, Graphics Engine, GPU, ARM926EJ-S, Cortex-M0+, power generation, supply, quad core, power consumption, autonomy,DMA, EDMA**

I. Introduction

It is known in bio-implants or battery critical applications or say in the event of grid fluctuations or partial collapse or unreliable grid ; in any of these conditions, the power consumption by amplifier or inverter, solar mppt or pwm, dc-dc boost or wind-turbine, motor-generator flywheel, meter and other smaller components involved in their own power consumption becomes an important factor.

In this paper, the power supply and consumptions in five processors is investigated for above scenarios and for other life-saving machines. The five processors namely SAMD21G18A, TMS570LS0432, AM3352BZCED60, AM1808EZCE and XCZU3EG-1SBVA484E is shown in Fig. 1. The choice of these processors is simply because these processors are in physical possession with the author (though he had practically worked on other processors also).

Fig.1(a) is SAMD21G18A soldered on Arduino MKR 1000 board which is mounted on adapter MKR2UNO expansion board. Fig.1(b) is TMS570LS0432, which is soldered on Hercules™ TMS570LS04 LaunchPad™ Development Kit. Fig.1(c) and Fig.1(d) are AM3352BZCED60 and AM1808EZCE respectively. Fig.1(e) is XCZU3EG-1SBVA484E soldered on Ultra96-V2-G single board computer with heatsink.

The paper is organized as - In Section II, Section III, Section IV, Section V, Section VI, SAMD21G18A single core, TMS570LS0432 dual core, AM3352BZCED60 single core, AM1808EZCE single core and XCZU3EG-1SBVA484E multicore processor/multiprocessor system on chip respectively.

II. SAMD21G18A

SAMD21G18A shown in Fig. 1(a) is a single-core 48 MHz AEC-Q100 Grade 1 (-40°C to 125°C) Arm Cortex-M0+ processor. For MKR2UNO Adapter, the operating current for both 3.3 V and 5 V pin is 700 mA. The operating voltage for SAMD21G18A is 1.62V - 3.63V, with maximum input suppy at 3.8V. The internal regulated voltage output is 1.2 V and it powers the core, memories, peripherals, FDPLL96M and DFLL48M. The maximum current into supply pin is 92 mA, maximum source current per cluster is 46mA, maximum sink current per cluster is 65mA and the maximum current out of ground pin is 130 mA. The rise rate of DC supply peripheral I/Os, internal regulator and analog supply is 0.1 V/μs. Under idle conditions, the minimum current consumption is 1.07 mA and the maximum 2.20 mA. At the time of any algorithm processing (which is of the interest of this paper), the minimum current consumption by CPU is 2.954μA, in general 3.10 mA and can easily consume 7 mA or more with complex algorithm. The RTC at 32 kHz consumes 7.4 μA but at 85°C, current consumption is 51.898 μA ; the watchdog timer with interrupt 'Early Warning(EW)' consumes 5.5 μA; analog comparator at 8MHZ 31.3 μA but at 85°C, current consumption is 70.533 μA ; Inter IC Sound at 12.288 Mhz with fractional digital phase-locked loop 49.152 MHz consumes 26.4 μA; DMAC 399.5 μA; Timer Counter for Control 0, Timer Counter for Control 1 and Timer Counter for Control 2 at 8 MHz consumes 180.3 μA, 167.5 μA and 95.5 μA respectively; USART serial communication at 8 MHz consumes 65.5 μA; SPI serial communication at 8 MHz consumes 64.6 μA ; USART serial communication at 8 MHz consumes 65.5 μA; USB v2.0 bus ON in suspend mode consumes 0.83 μA; USB v2.0 bus in active running

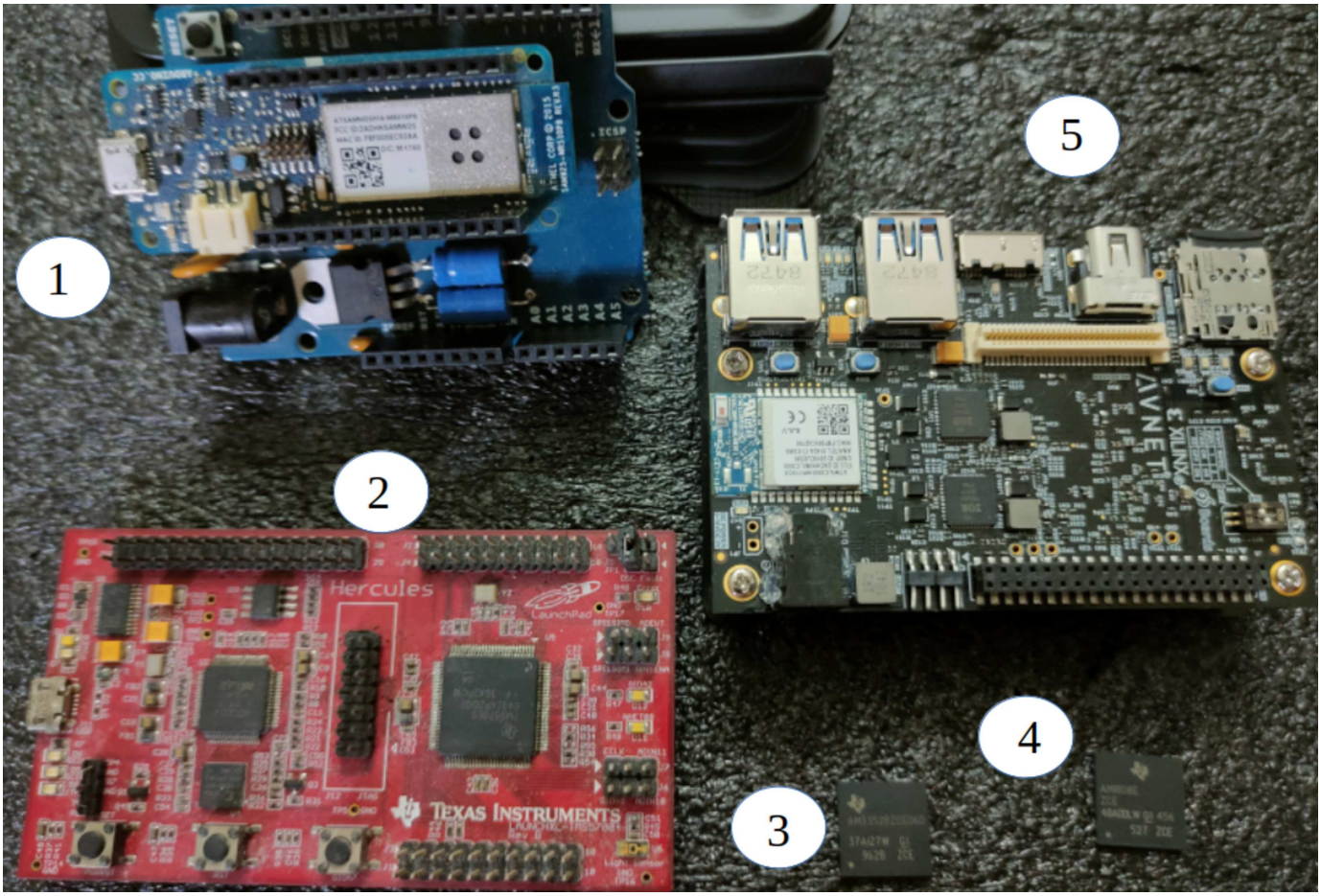

Fig. 1. (a) SAMD21G18A (b) TMS570LS0432 (c) AM3352BZCED60 (d) AM1808EZCE (e) XCZU3EG-1SBVA484E

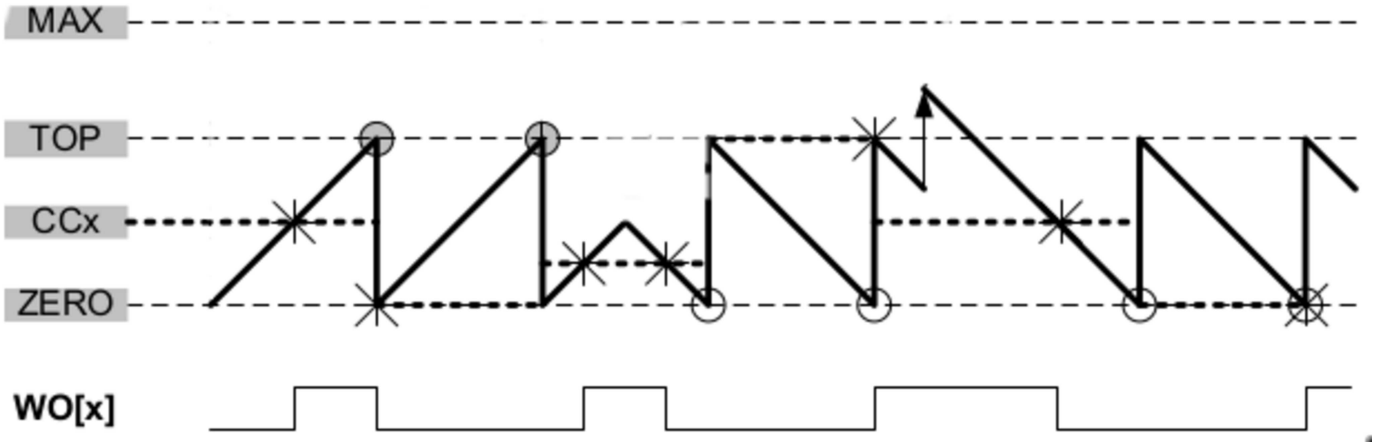

Fig. 2. TC Normal PWM

mode 10.3 mA.

The 12-bit ADC can run at 30 kHz upto 2100 kHz with sample rates for single-shot and free running 5 ksps upto 350 ksps in 250 ns but if DAC or temperature sensor is used as input, then consumption is 3μA and 10μA respectively. but at 85°C, current consumption is μA .

The package thermal resistance, Junction-to-ambient is 63.6°C/W and Junction-to-case thermal resistance is 12.2°C/W.

A. DMA

SAMD21G18AG18AG18A can use DMA for data transfer from peripheral-to-peripheral, peripheral-to-memory, memory-to-peripheral or memory-to-memory. This processor's has 12 DMA Controllers (DMAC) which consists of Direct Memory Access (DMA) engine and a Cyclic Redundancy Check (CRC) engine, and are 12 independent tranfers. Of these 12 channels, at a time only one channel remains active; and interupts and events could be generated only afterwards if required. The CRC engine find whether data transferred is corrupted or not and is accomplished by either CRC-16 (CRC-CCITT) polynomial or CRC-32 (IEEE 802.3) polynomial.

The DMAC has three Advanced High-performance Bus(AHB) host bus interfaces namely data transfer bus, descriptor fetch bus and write-back bus. The DMAC also has one Advanced Peripheral Bus(APB) client interface or AHB client called as AHB/APB Bridge bus, which is based on AMBA APB4 and thus supports even sparse data transfer. In a single block transfer upto 256 KB can be transferred. The data transferred by the DMAC is categorized in beat, burst, block(1 to 64k beats) and transaction transfer. The steps to use and configure DMA are as :

1) The Generic Clock Generator, GCLK_IO[7:0] is multiplexed with I2S/Serial Clock/Host Clock/I2S Word Select or TDM Frame Sync is configured. The division factors can be 512, 131072 or 64 which is accomplished by 8-bits, 16-bits and 5-bits respectively in 32-bit GENDIV[0:31], and thus the GCLK Generator ID can be 0x00 - 0x08.
2) The clock source must be selected in SRC[4:0] from XOSC oscillator, Generator input pad, Generic clock generator 1, OSCULP32K oscillator, OSC32K oscillator, XOSC32K oscillator, OSC8M oscillator, DFLL48M, FDPLL96M; and then enabling generic clock generator in the 32-bit GENCTRL. The generic clock is then configured in 16-bit CLKCTRL.
3) An AHB clock, CLK_DMAC_AHB and DMAC bus clock, CLK_DMAC_APB are enabled in Clock Mask register. The 32-bit Descriptor Memory Section Base Address, 0x34(offset) and 32-bit Write-Back Memory Section Base Address, 0x38(offset) tell DMAC of transfer descriptors.
4) The Nested Vectored Interrupt Controller(NVIC) supporting 32 interrupt lines IRQ[31:0], having address 0xE000E100 is enabled in 32-bit Interrupt Clear Enable Register, NVIC_ICER by CLRENA bit and 32-bit Interrupt Set-Enable Register, NVIC_ISER by SETENA bit. Thus, we get even a 24-bit system timer,SysTick clocked by CLK_CPU and has its own control and status register(SYST_CSR, 0xE000E010), counter reload value register(SYST_RVR, 0xE000E014), counter current value register(SYST_CVR, 0xE000E018) and calibration value register(SYST_CALIB, 0xE000E01C).
5) After selecting the channel in CHID, 0x3F(offset); Trigger Action bit,TRIGACT[1:0]; Trigger Source, TRIGSRC[5:0] in CHCTRLB, 0x44(offset); and Beat Size, BEATSIZE[1:0] in 16-bit Block Transfer Control register, the CTRL.DMAENABLE, CHCTRLA.ENABLE are set to 1. The number of beats are selected in 16-bit Block Transfer Count, BTCNT; source address in 32-bit Block Transfer Source Address, SRCADDR; and destination address in 32-bit Block Transfer Destination, DSTADDR.

The synchronization delay is the range $5 \times P_{GCLK} + 2 \times P_{APB} < D < 6 \times P_{GCLK} + 3 \times P_{APB}$

B. Pulse Width Modulation

Twelve Pulse-Width Modulation(PWM)channels are achieved from five Timer/Counters(TC) and four instances of Timer/Counter for Control, TCC[0:3]. The 16-bit TC provides upto two single-slope PWM channels. The 16-bit TCC gives upto two PWM channels and 24-bit TCC gives eight PWM channels, which can be single-slope, dual-slope pulse-width modulation with half-cycle reload capability or dual-slope critical PWM. The synchronization is done by setting software reset and enable bits to 1 in Control A(CTRLA) register(offset, 0x00); CTRLBCLR(offset, 0x04), CTRLBSET(offset, 0x05), CTRLC(offset, 0x06), PER(offset, 0x14) holding Period Buffer PERBUF; Channel x Compare/Capture with offset 0x18 + $x \times$ 0x01 ($x \in [0, 1]$) and COUNT(offset, 0x10).The RETRIGGER(0x1) in CTRLBSET and CTRLBCLR triggers and one-shot on counter and will wrap around and continue counting on an overflow/underflow condition, which are executed on next prescaled GCLK_TC (0x1B or 0x1C or 0x1D). If TC is in 8-bit, PER = TOP. If TC is in 16-bit or 32-bit mode, then Period Value, PER = Compare Channel x (CCx) register value.

Fig. 2 and Fig. 3 shows the single slope PWM generation using Timer/Counters(TC) Normal PWM (NPWM) and Match PWM(MPWM) respectively. The clock CLK_TCx_APB according to TC number is enabled. In Fig. 2 - Fig. 6, grey circle is 'clear' update, white circle is 'reload' update and $*$ denote 'match'.

For single-slope PWM, TOP and CCx controls period time(T) and duty cycle(D) respectively. The digital output signal (Waveform output), WO[1:0] is then set

Exact Resolution, $R_{NPWM} = \dfrac{log(TOP+1)}{log2}$

The PWM frequency, $f_{NPWM} = \dfrac{f_{GCLK_TC}}{N(TOP+1)}$,

$N = \{2^0, 2^1, 2^2, 2^3, 2^4, 2^6, 2^8, 2^{10}\}$
$= \{1, 2, 4, 8, 16, 64, 256, 1024\}$

In Fig.3, Match PWM (MPWM) is shown where the output of WO[1] depends on CC1 and on every overflow/underflow,

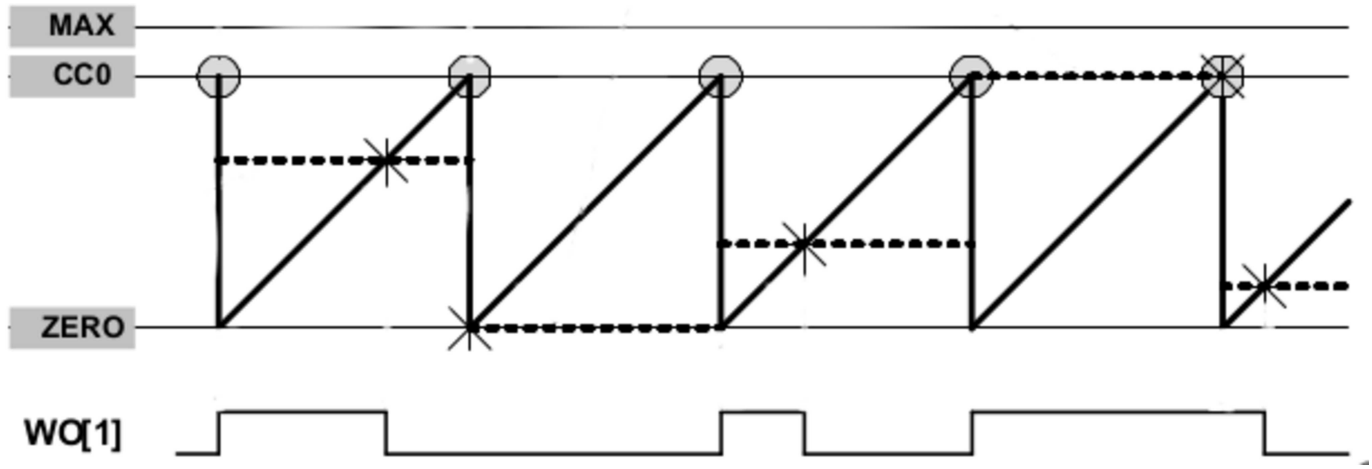

Fig. 3. TC Match PWM

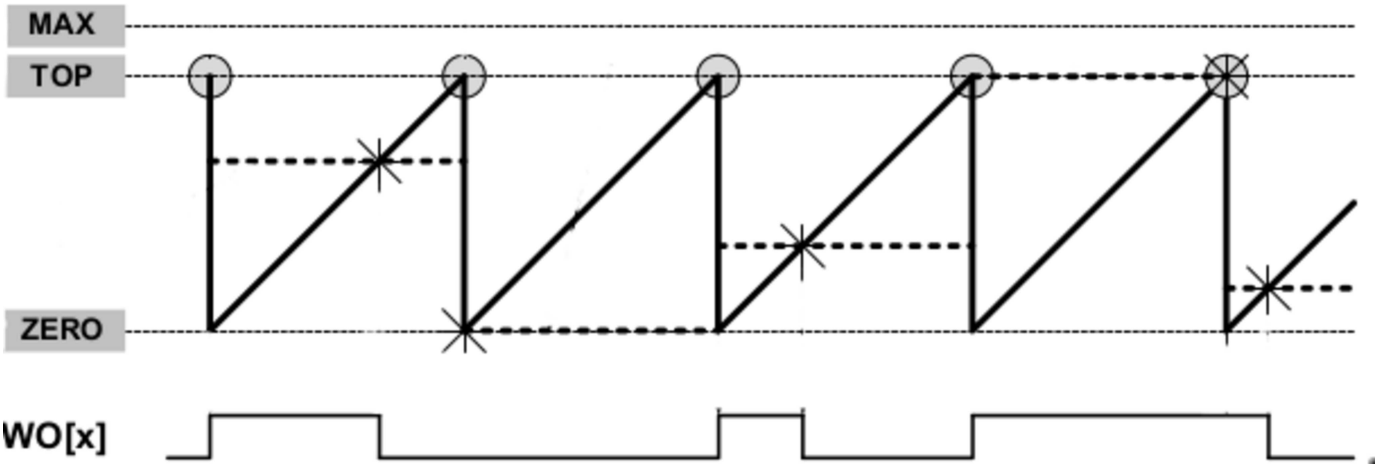

Fig. 4. TCC Single Slope PWM

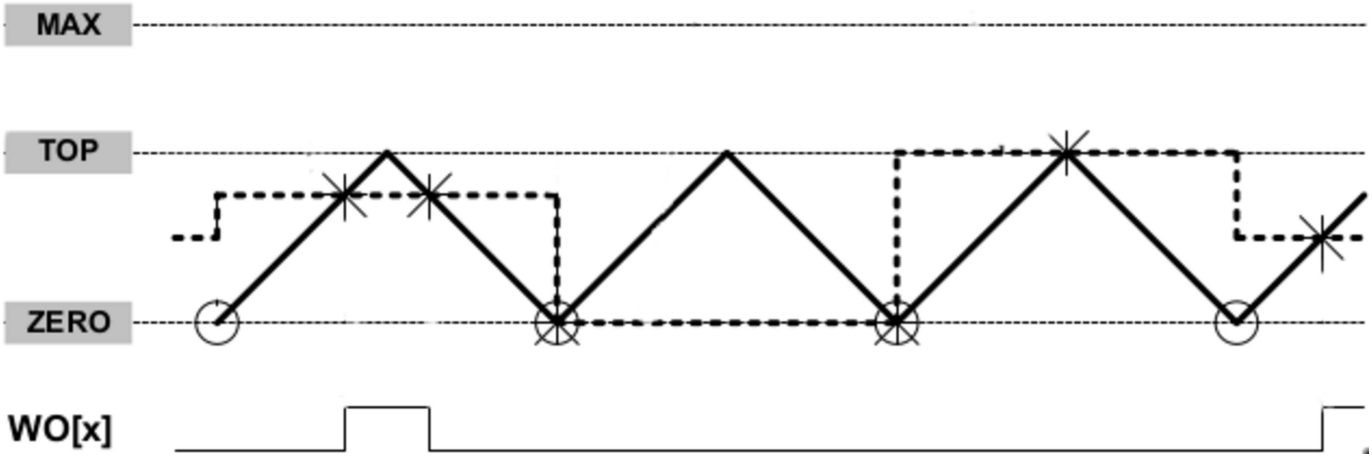

Fig. 5. TCC Double Slope PWM

a one-TC-clock-cycle negative pulse is put out on WO[0].

If the PWM is generated using TCC[0:3], then clock CLK_TCCx_APB according to TCC[0:3] number is enabled. The Single-Slope PWM Operation is same as using TC, shown in Fig. 4. For dual-slope PWM shown in Fig. 5 and Fig. 6, PER controls TOP and CCx controls duty cycle.

Exact resolution, $max(R_{TCC_{DSPWM}}) < max(R_{NPWM})$

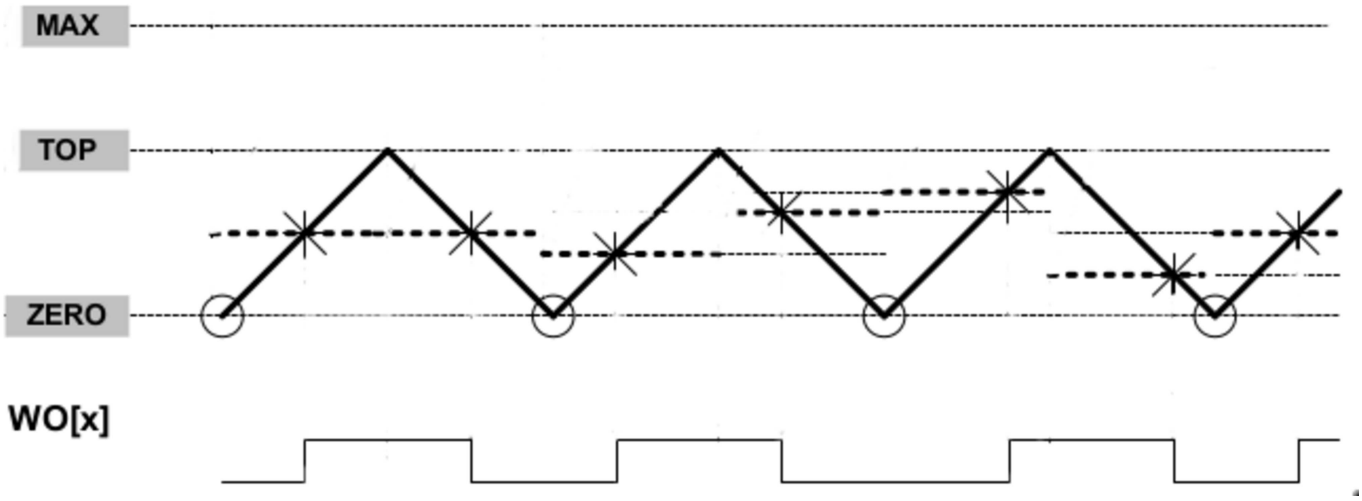

Fig. 6. TCC Double Slope Critical PWM

or, $\frac{log(PER+1)}{log2} < \frac{log(TOP+1)}{log2}$

If non-aligned centered pulses have to be generated, then critical mode shown in Fig. 6, of dual-slope PWM can be used.

III. TMS570LS0432

The TMS570LS0432 processor, shown in Fig. 1(b), is a 80 MHz 32-bit RISC real-time computing ARM Cortex R4 microprocessor based on ARMv7-R,in which dual CPUs run in lockstep with full duplex VBUSM Switched Central Resource(SCR) Controller and the outputs of two CPUs are compared on each CPU clock cycle. The packaging of TMS570LS0432 is in LQFP (Low-profile Quad Flat Package) with 100 balls and dimension 2.56 mm^2, with efficiency of 1.66 DMIPS/MHz in 8-stage pipeline, thus providing upto 1.66 $\times$ 80 = 132.8 DMIPS $\approx$ 132 DMIPS. The nominal voltages for core digital logic is 1.2 V whereas I/O, Multibuffered ADC and flash pump need 3.3V. The input hysteresis is 180 mV and max. voltages of multibuffered A-to-D high-voltage and low-voltage reference source are 3.6V and 0.1 V respectively. The input and output capacitance of 2 pF and 3 pF respectively. The switching time with 15 pF for 8 mA pin is 2.5 ns, for 4 mA pin is 5.6 ns, for 2 mA pin is 8 ns. The switching time with 150 pF for 8 mA pin is 12.5 ns, for 4 mA pin is 23.2 ns, for 2 mA pin is 33 ns. The input clamp current is -40 mA to 40 mA with maximum current consumption $\approx$ 531 mA. The CPU self-test built-in self-test LBIST with 45 MHZ consumes max. of 145 mA and last for $<$ 10 ms. The programmable built-in self-test (PBIST) with 80 MHZ consumes max. of 135 mA and last for $<$ 10 ms. The main oscillator frequency is between 5 MHZ and 20 MHZ which is used by 32-bit CPU clock, GCLK in phase with system module clock, HCLK.

A. DMA

DMA type 32-bit and 64-bit transactions is achieved through High End Timer Transfer Unit (HET-TU or HTU) which transfers data between N2HET(Next Generation High-End Timer) RAM and RAM buffers located in the main memory address range. For each of the 8 double control packets, there is one shot mode or circular mode in single buffer implementation and auto switch buffer transfer modes and can be in constant addressing mode or post-increment addressing mode. HTU has Memory Protection Unit (MPU), control, FIFO. This eliminates time consuming CPU accesses to N2HET RAM. If the HTU memory protection is disabled, full 4 GB address range can be accessed without exception. The HET-TU RAM frame size is 128 KB, actual size is 1 KB with address 0xFF4E_0000 to 0xFF4F_FFFF.

B. Pulse Width Modulation

The timer module used to implement PWM is called as High-End Timer (N2HET), an advanced intelligent timer module which allow greater accuracy. This is implemented using two 25-bit registers and three 32-bit registers and each 96-bits wide N2HET instruction aligned to a 128-bit boundary in Very Long Instruction Word (VLIW) format. The 32-bit N2HET[0:31] is pulldown, programmable, 20μA. The high resolution hardware timers operate with frequency multiples between 2 and 128 times loop resolution period. The N2HET peripheral control register has frame and actual size of 256B with address 0xFFF7_B800 to 0xFFF7_B8FF. The N2HET RAM frame size is 128 KB, actual size is 16 KB with address 0xFF46_0000 to 0xFF47_FFFF.

This is called N2HET because of enhancements which earlier timer module was unable to perform viz., eight new instructions,signed and unsigned arithmetic conditions have

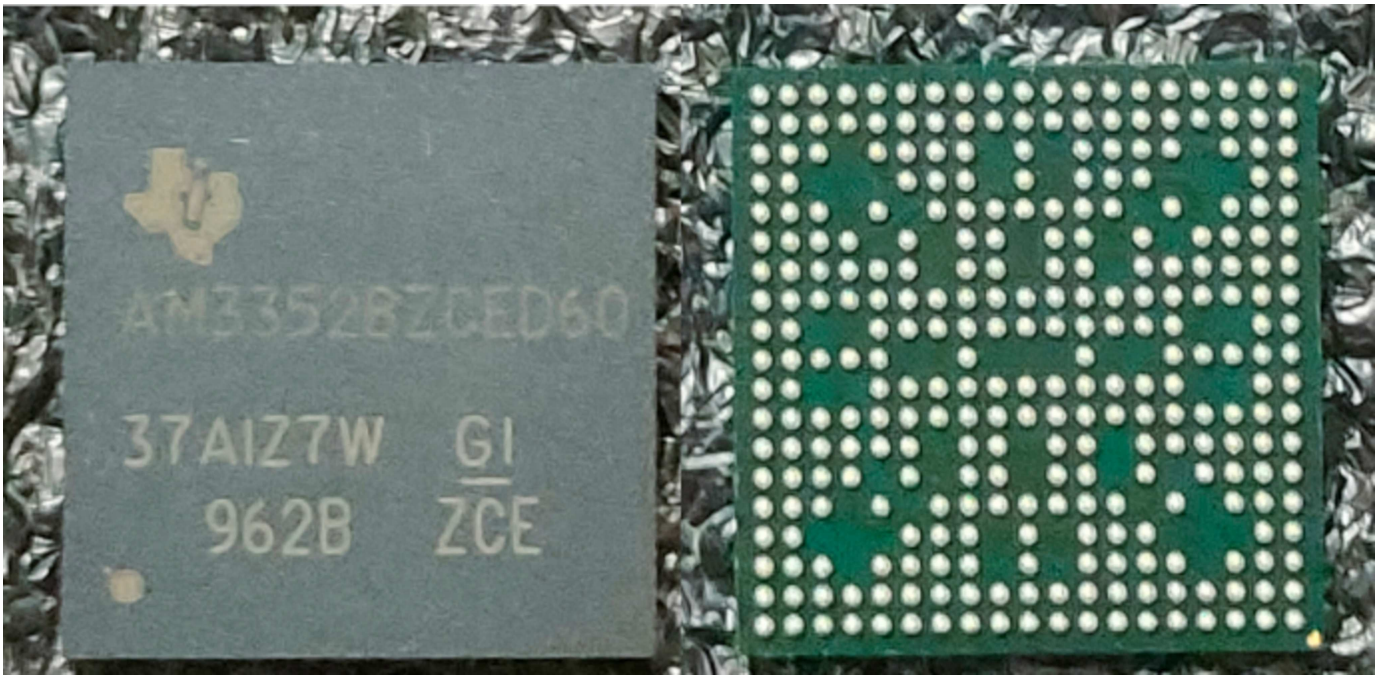

Fig. 7. AM3352BZCED60

branch instruction, additional 32-bit temporary working registers, new Interrupt registers, parity error detection; 9 bit next, conditional and remote addresses ; 25 bit loop resolution data and 7 bit high resolution data fields; virtually extend counter width employing multi-resolution scheme.

IV. AM3352BZCED60

The AM3352BZCED60 processor, shown in Fig. 7, is a single core 1 GHz 32-bit RISC ARM microprocessor based on ARM Cortesx A-8 with 298 balls and dimension 1.69 mm^2. This is in nFBGA (New Fine Pitch Ball Grid Array) packaging which has reduced height of solder bumps, pitch of 0.5mm, Die 1 is 10.6×8.2 mm^2, Die 2 is 8.1×7.7mm^2. Using the known finite element analysis and statistics method,reliabilty had been determined by the manufacturer itself. A 2D finite element model (FEM) is used for 2D plain strain elastoplastic analysis which calculate the thermomechanical plastic strains in the solder joints. The highly accelerated temperature and humidity stress test with 600 cycles and 1000 cycles is 0/77. This processor is manufactured by Texas Instruments and marketed as Sitara ARM microprocessor. For DMA transfer, this processor uses on chip Enhanced Direct Memory Access Controller 3(EDMA3), which has 64 independent DMA Channels, 8 Quick DMA (QDMA)Channels, 64 Event Inputs, 8 Interrupt outputs, 3 event queues, 256 PaRAM entries. The DMA and PWM as such is similar to AM1808EZCE, explained in the next Section V.

V. AM1808EZCE

The AM1808EZCE processor, shown in Fig. 8, is a single core 375 MHz and 456 MHz,32-bit RISC ARM microprocessor based on ARM926EJ-S with 361 balls and dimension 1.69 mm^2. This ARM926EJ-S is based on ARM Jazelle® Technology and is ARM9 + Enhanced + Jazelle - Synthesizable, which executes Java bytecode in hardware as direct bytecode execution and implements the basic ARM9TDMI pipeline with add support for ARMv5TE architecture, thus 16 bit Thumb + JTAG Debug + fast Multiplier + enhanced ICE. The packaging is same as AM3352BZCED60 processor, that is, nFBGA (New Fine Pitch Ball Grid Array) packaging with reduced height of solder bumps, pitch of 0.5mm, Die 1 is 10.6×8.2 mm^2, Die 2 is 8.1×7.7mm^2. This processor is also manufactured by Texas Instruments and marketed as Sitara ARM microprocessor.

The input current with internal pullup resistor is 310μA and the low-level output current is 6 mA. The clamp current which flows through the I/O's internal diode protection cells is limited to maximum of $\pm$20 mA.

The thermal resistances of junction-to-case are 7.6°C/W, junction-to-board 11.3°C/W and junction-to-free air 23.9°C/W.

A. DMA

For DMA transfer, this processor uses on chip Enhanced Direct Memory Access Controller 3(EDMA3), which has three fully orthogonal transfer controllers (EDMA3_m_TCn), 64 independent DMA Channels, 16 Quick DMA (QDMA)Channels, 2 channel controllers (EDMA3_m_CC0) and 256 parameter RAM (PaRAM) entries. The PaRAM structure supports circular buffering, channel chaining and

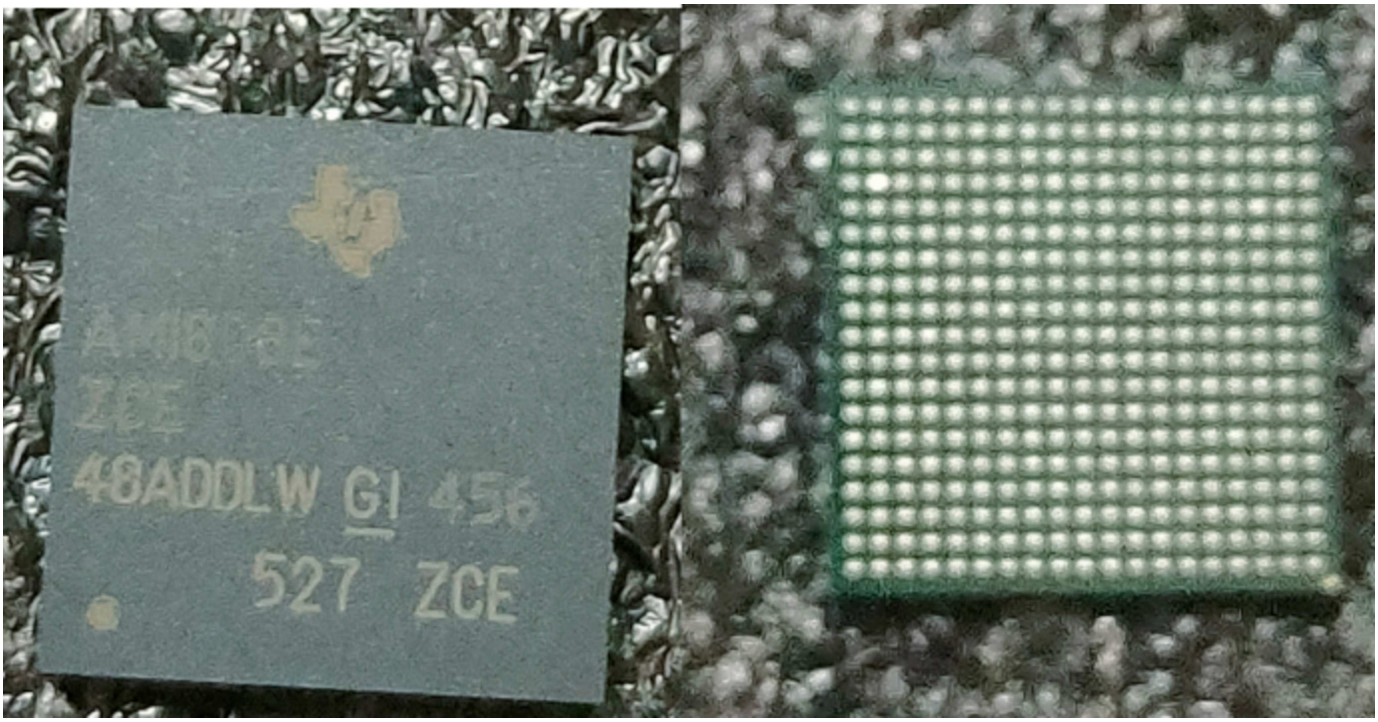

Fig. 8. AM1808EZCE

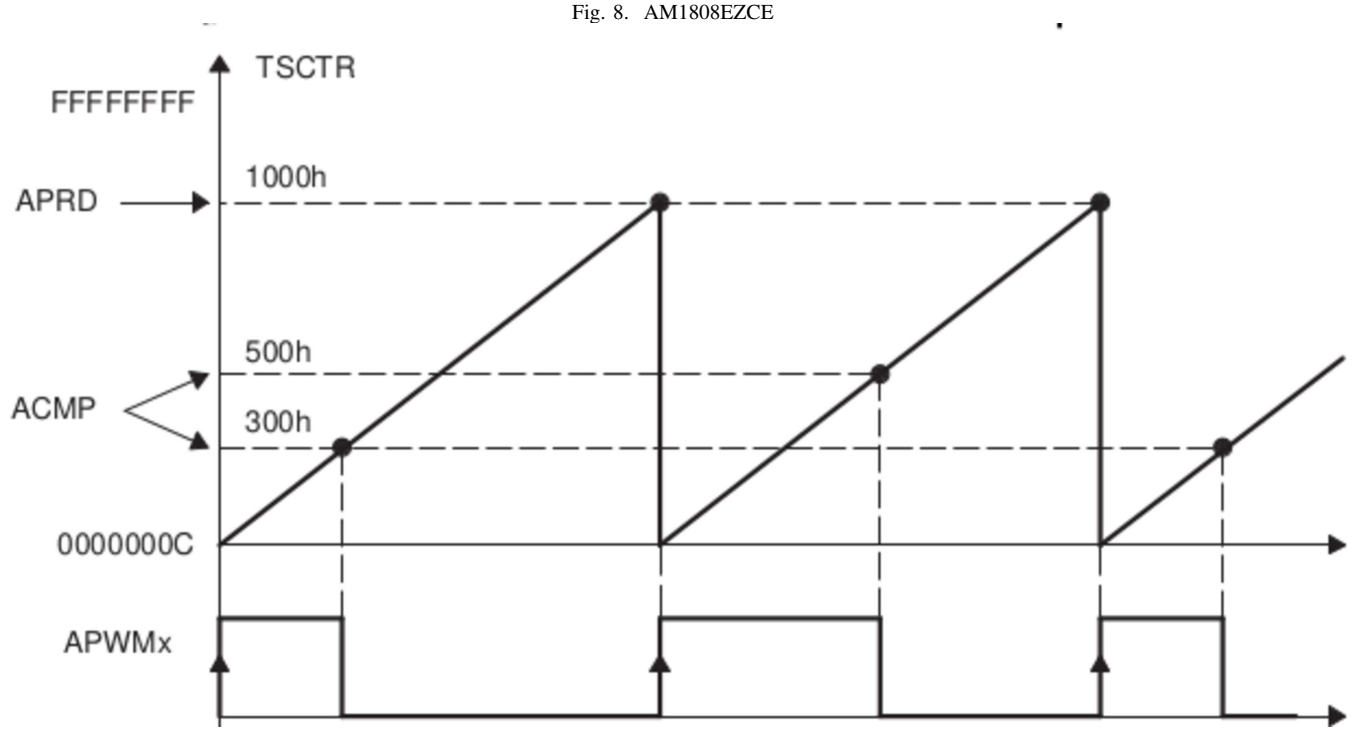

Fig. 9. Auxiliary PWM using eCAP in AM1808EZCE

linking.

There are interrupts assignments in ARM interrupt controller (AINTC) viz., EDMA3_0_CC0_INT0, EDMA3_0_CC0_ERRINT and EDMA3_0_TC0_ERRINT, which are sourced from EDMA3_0 Channel Controller 0 Shadow Region 0 Transfer Completion Interrupt, EDMA3_0 Channel Controller 0 Error Interrupt and EDMA3_0 Transfer Controller 0 Error Interrupt respectively. The EDMA3_0_TC0 and EDMA3_0_TC1 have default master priority of 0 in MSTPRI1 (01C1 4114h). The EDMA3_1_TC0 has default master priority of 4 in MSTPRI1.

Similarly, we have 7 more interrupts in AINTC for EDMA3 Transfer Completion namely EDMA3_0_CC0_INT1, EDMA3_0_CC0_INT2, EDMA3_0_CC0_INT3, EDMA3_1_CC0_INT0, EDMA3_1_CC0_INT1, EDMA3_1_CC0_INT2 and EDMA3_1_CC0_INT3. And there are three more error interrupts EDMA3_0_TC1_ERRINT, EDMA3_1_TC0_ERRINT and EDMA3_1_CC0_ERRINT.

The transfer controllers EDMA3_0_TC0 and EDMA3_0_TC1 have FIFIOSIZE of 128 bytes, BUSWIDTH of 64 bits, Destination FIFO register number 4. The burst size for these transfer controllers can be 16 bytes(1h), 32 bytes(2h) or 64 bytes(3h) which is configured in chip configuration 0 register, CFGCHIP0. EDMA3 transfer uses three dimensions. In an A-synchronized transfer each EDMA3 transfer contiguous bytes or one array of ACNT bytes(offset, 8h). Arrays are separated by 2s complement of 16-bit signed value Source B Index and 2s complement of 16-bit signed value Destination B Index (offset, 10h). Frames are separated by 2s complement of 16-bit signed value Source C Index and 2s complement of 16-bit signed value Destination C Index (offset, 18h). In a AB-synchronized transfer, each EDMA3 transfer 2 dimensions, that is BCNT arrays of ACNT bytes. When EDMA3 uses 3 dimensions, then it initiates transfer of CCNT (offset, 1Ch) frames of BCNT arrays of ACNT bytes.

B. Pulse Width Modulation

There are four modules using which PWM can be generated viz.eCAP (enhanced capture), ePWM (enhanced pulse-width modulator), HRPWM and eHRPWM (enhanced high-resolution pulse-width modulator).

The auxiliary pulse-width modulator (APWM), shown in Fig. 9, a single channel 32-bit PWM can be generated using eCAP module where CAP1 (offset, 8h), CAP2 (offset, Ch), CAP3 (offset, 10h) and CAP4 (offset, 14h) becomes active period, compare, period and capture shadow registers respectively.

The ePWM module gives two PWM outputs EPWMxA and EPWMxB, which can be single-edge, dual-edge symmetric or dual-edge asymmetric. The trip-zone asynchronous input signals,$\overline{TZ1}$ to $\overline{TZn}$ can be configured as One-Shot (OSHT) trip-zone or Cycle-by-Cycle (CBC) in 16-bit trip-zone select, TZSEL(offset, 24h). The duty cycle can be selected with chopping clock in 16-bit PWM-chopper control register (PCCTL) with 1/8 (0h), 2/8(1h), 3/8(2h), 4/8(3h), 5/8(4h), 6/8(5h),7/8(6h), which is 12.5%), 25.0%, 37.5%, 50.0%, 62.5%, 75.0%, 87.5% respectively.

There is also a high-resolution PWM (HRPWM) submodule which can be configured in registers HRPWM Configuration HRCNFG, Time-Base Phase High-Resolution TBPHSHR and Counter-Compare A High-Resolution CMPAHR. The differences in bits and % using regular or high resolution vs PWM frequency is shown in Table I.

In eHRPWM (enhanced high-resolution pulse-width modulator) mode, multiple PWM outputs can be achieved, viz., with single-edge operation two independent PWM outputs, with dual-edge symmetric operation two independent PWM outputs, with dual-edge asymmetric operation one independent PWM output.

TABLE I
PWM FREQUENCY VS REGULAR & HIGH RESOLUTION

S.No.	PWM Frequency	Regular Resolution		High Resolution	
		Bits	%	Bits	%
	kHz				
1	20	12.3	0.0	18.1	0.000
2	50	11.0	0.0	16.8	0.001
3	100	10.0	0.10	15.8	0.002
4	150	9.4	0.20	15.2	0.003
5	200	9.0	0.20	14.8	0.004
6	250	8.6	0.30	14.4	0.005
7	500	7.6	0.50	13.8	0.007
8	1000	6.6	1.0	12.4	0.018
9	1500	6.1	1.5	11.9	0.027
10	2000	5.6	2.0	11.4	0.036

VI. ULTRA96-V2-G XCZU3EG-1SBVA484E

The Ultra96-V2-G shown in Fig. 1(e) with silicon core number XCZU3EG-1SBVA484E is different from any of the processors mentioned in this article as it is single board computer (SBC) multiprocessor by AMD (earlier Xilinx) Zynq UltraScale+ MPSoC ZU3EG SBVA484 manufactured by AVNET, has core architecture of dual core Cortex-R5F and quad core Cortex-A53 with 484 I/O pins, 82 I/O Buffer, 70560 Look-up Table (LUT) elements, 141120 flip flops and form factor of 85mm $\times$ 54 mm. Each core of Cortex-R5F is Arm v7 architecture-based 32-bit dual real-time processing unit (RPU) with performance upto 600 MHz and floating-point unit ARM VFPv3 instruction set with 32-bit master advanced eXtensible interface (AXI) peripheral interface for low-latency device memory type access to the interrupt controller. And each core of Cortex-A53 is Arm v8 architecture-based 64-bit 1.5 GHz 13800 DMIPS Application processing unit (APU) with 128-bit AXI coherency extension (ACE) master interface to CCI(Cache coherent interconnect).

As this is a multi-core multi-processor which is FPGA based, its architecture is being mentioned in detail. The common block diagram showing the features of Zynq UltraScale+ processing system which includes PS Interconnect, AXI interconnect, System Protection Units,PS-PL AXI Interfaces, is explained in subsection 'A' and shown in Fig. 10.

The features like Cortex R5F RPU, Cortex A8 APU, Cortex A8 GPU Geometry processor, Cortex A8 GPU Pixel processor, RTC controller functional block diagram, DMA & PWM and clock settings are also explained in below subsections.

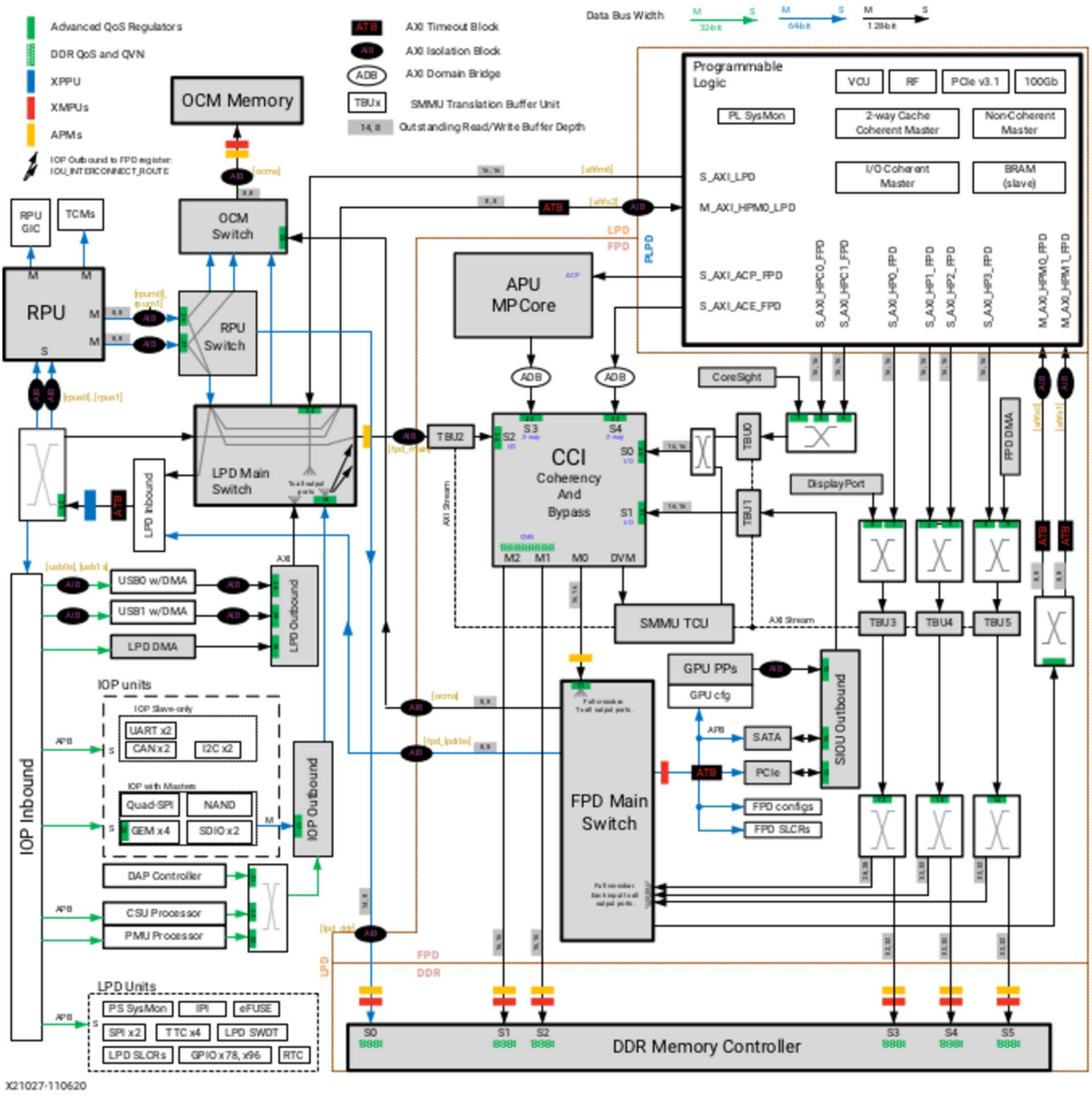

Fig. 10. Block Diagram of Zynq UltraScale+ Processing System Source : AMD Xilinx

The intellectual property core revisions used in this paper for Cortex-R5F RPU Core is ARM r1p3, Cortex-A53 APU Core is ARM r0p4-50rel0, Crypto APU Core is ARM r0p4-00rel0, Mali-400 GPU Graphics is ARM r1p1-00rel2, CCI-400 CI Coherent Interconnect is ARM r1p3-00rel0, NIC-400 AXI Interconnect is ARM r0p2-00rel0, GIC-400 APU GIC Interrupts is ARM r0p1-00rel0, PL390 RPU GIC Interrupts is ARM r0p0-00rel2, SoC-400 CoreSight Debug is ARM r3p1-00rel0, QoS-400 AXI Interconnect QoS is ARM r0p2-00rel0, SMMU-500 SMMU (System memory management unit) is ARM r2p1-00rel1, STM-500 CoreSight STM is ARM r0p1-00rel0, GEM Ethernet Controllers is Cadence r2p03, GEM Ethernet GXL is Cadence r1p06f1,GEM Ethernet RGMII is Cadence r1p04, I2C Controllers is Cadence r114_f0100_final, TTC Timer/Counters is Cadence r2, UART Controllers is Cadence r113, SPI Controllers is Cadence r109, DDR Memory Controller is Synopsys 2.40a-lp06, GDSII DDR Memory PHY is Synopsys1.40a_patch1,

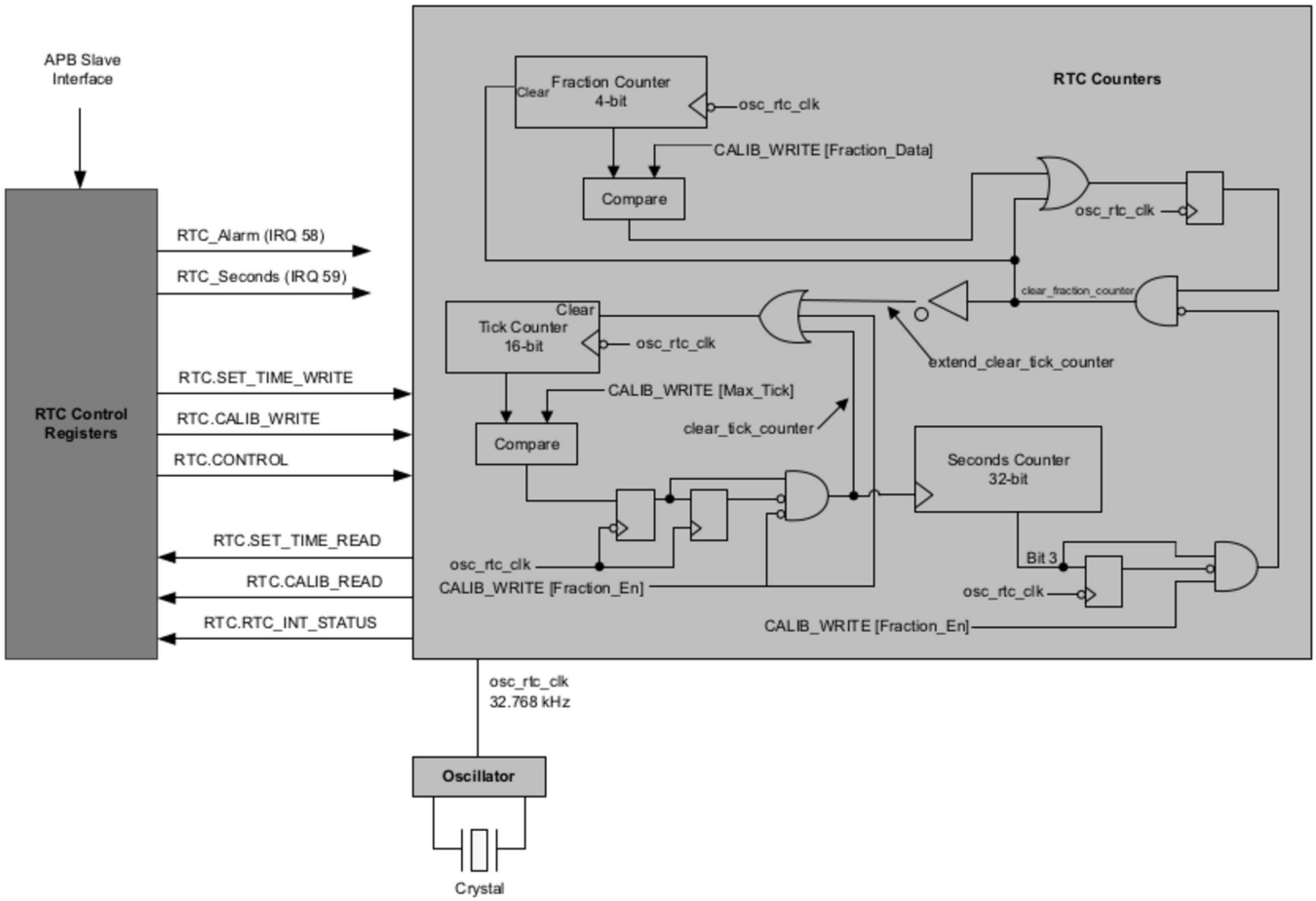

Fig. 11. RTC Controller Functional Block Diagram Source : AMD Xilinx

USB 3.0 Controllers is Synopsys 2.90a, SD/SDIO/eMMC Controllers is Arasanver1p48_140929m, NAND Controller is Arasanv3p9_140822, LPD DMA & FPD DMA Units is Northwest Logic1.13, SATA Controller is CEVA FA13 and Neon APU Core is ARM r0p4-00rel0.

A. Common Block Diagram

Fig. 10 shows the complete block diagram which comprises of basically two blocks - processing system (PS) and programmable logic (PL). The PS block acts as standalone SoC & consists-application processing unit (APU), real-time processing unit (RPU), graphics processing unit (GPU) and Video control unit (VCU).

Majority of registers are XPPU (Xilinx peripheral protection unit) protected, SIOU controller registers are XMPU (Xilinx memory protection unit) protected and secure registers are hardware protected. The secure and non-secure AXI transactions are accomplished by TrustZone - APU MPCore/L2, GIC, APU system counter, CCI_REG control register, CCI GPV, SMMU TCU APB , SMMU TBU AXI, APB/AXI interface, DMA, RPU R5_0/1, RPU TCMs, FPD/LPD Secure SLCR, LPD CSU/PMU, eFUSE/BPD/PS_SYSMON, CoreSight, LPD IOP, LP slave interfaces on APB, TTC(0:3), LPD GPU/SATA/DP/PCIe, LPD FP slaves APB, DDR RAM and OCM.

The supported total memory density is 34 GB (maximum) with component memory density of 0.5, 1, 2, 4, 6, 8, 12, 16 Gb per die. DDR memory controller implements QoS policy to handle Video/isochronous(real-time, fixed bandwidth, fixed maximum latency), low latency(high-priority) and best effort high-latency(low-priority) traffic classes by prioritizing in four major blocks - an AXI port interface, port arbiter(PA), DDR controller(DDRC) and APB register block. The XPI converts AXI bursts into DRAM r/w ; the logical content addressable memory is used by scheduling algorithms. The on-chip memory (OCM) contains 256 KB of RAM which is divided into 64 blocks (4 KB each).

1) Power Domains: There are four power domains viz., Low-power domain (LPD), Full-power domain (FPD), PL power domain (PLPD) and battery power domain (BPD),

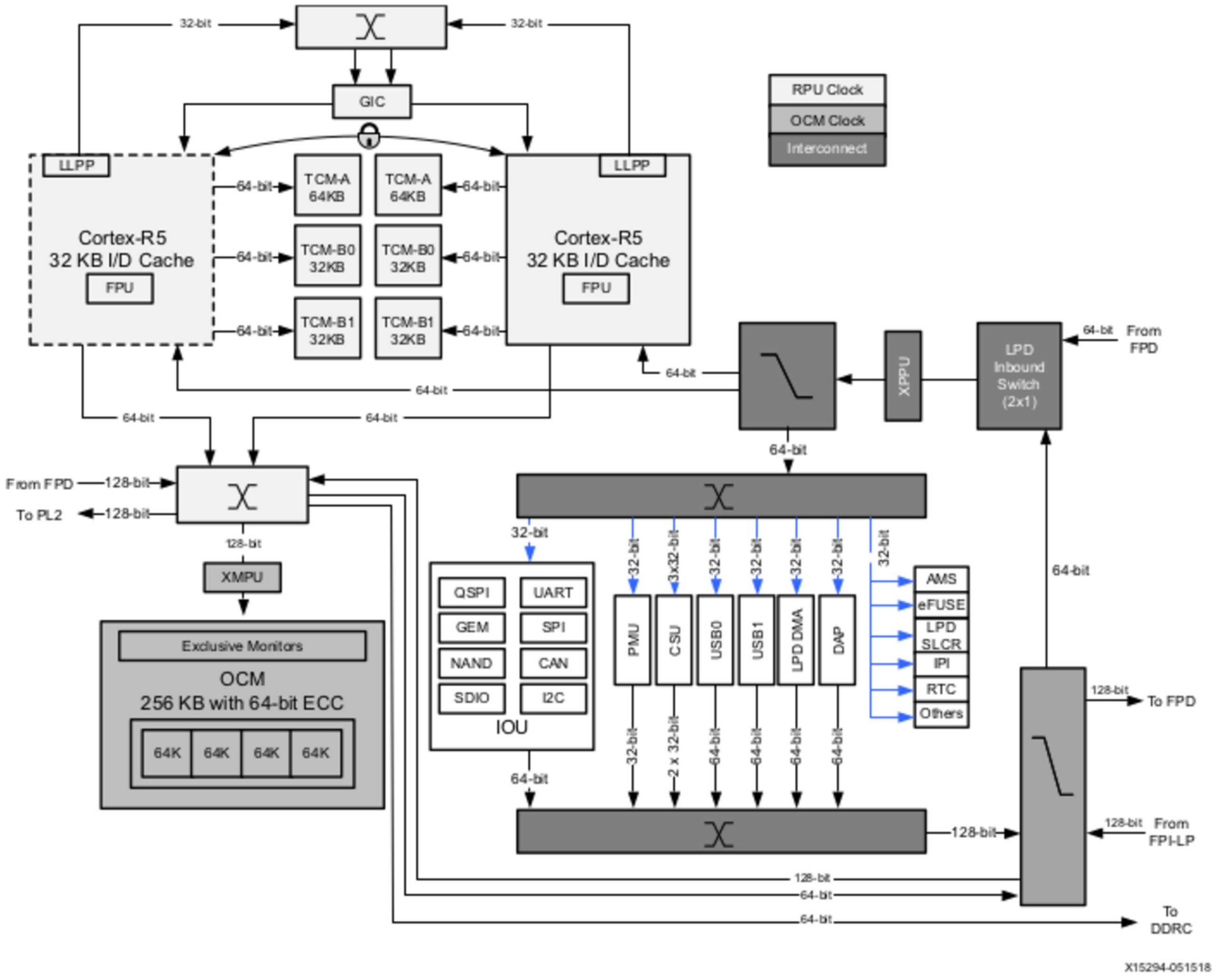

Fig. 12. Cortex R5F RPU Source : AMD Xilinx

which can be individually isolated. LPD main switch and 128-bit FPD main switch can be seen in big grey boxes.

In FPD, we have APU Debug, APU MP Core (SCU,GIC,CCI, L2 Cache RAM,CPU0, CPU1, CPU2 & CPU3), Interconnect and SCLR (DMA, PCIe, SATA, DisplayPort, GPU Pipeline), GPU PP0, GPU PP1, PHY, DDR Memory Controller and there is PL-FPD isolation wall.

In LPD, we have Interconnect and SCLR (PS System Monitor, CSU, PMU, PS TAP, eFuse, IOP, IPI, DMA, USB0, USB1), OCM Control (Bank0, bank1, bank2 and bank3), RPU MPCore (GIC, ETM, TCM A0, TCM A1, TCM B0, TCM B1), PL and RPU Debug, ARM DAP, PCAP, PCAP-LPD isolation wall and PL-LPD isolation wall.

In PL Power Domain (PLPD), we have PL fabric, PL configuration, PL TAP, PL AXI Interconnect, BRAM, VCU H.265, H.265, PL System monitor, I/O(HP, HD), SerDes, 100 Gb/s Ethernet, DSP, LUT, clocks, PCIe Gen3, PCIe Gen 4 and 150 Gb/s interlaken.

The high-performance I/O consists of PLPD and its blocks, DDRIOB, PS GTR/GHY transceivers, MIO0, MIO1 and MIO2. The high-speed serial I/O, SIOU peripherals share four GTR transceivers in PS/FPD and USB controller in LPD. The GTY transceivers transfer data up to 32.75 Gb/s.

Fig. 11 shows RTC, functional block diagram of real time clock (RTC); dark grey is LPD and light grey is BPD.

There are separate system watchdog timers for FPD interconnect, LPD interconnect and CSU/PMU (configuration security unit/platform management unit) interconnect.

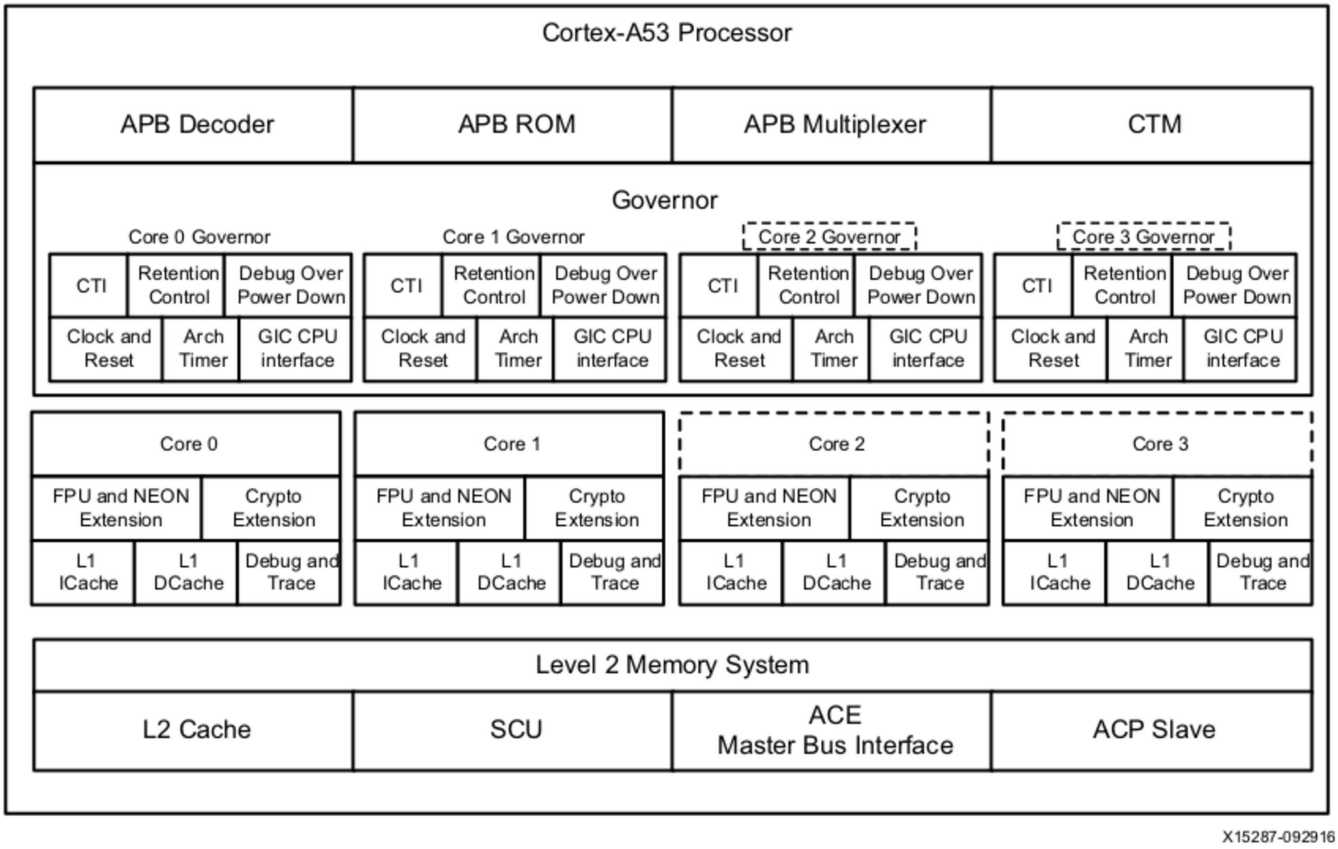

Fig. 13. Cortex A8 APU Source : AMD Xilinx

B. Cortex R5F RPU

As can be seen in Fig. 12, RPU consists of two Cortex R5F processors for real-time processing which can operate independently or in lock-step together. RPU GIC has 160 shared peripheral interrupts divided into five, 32-bit APB registers. Each core of R5F RPU has low-latency tightly-coupled memories (TCMs) which contain two 64-bit wide 64 KB memory banks on ATCM port holding interrupt or exception code and BTCM port holding block of data. This results in predictable instruction execution and predictable data load/store timing.

C. Cortex A8 APU

As can be seen in Fig. 13, APU consists of four Cortex A53 MPCore processors where ech core has Governor controlling CTI (CoreSight cross-trigger interface), retention control, debug over power down, clock & reset, arch timer and GIC(generic interrupt controller) CPU interface, FPU & NEON extension, 32K L1 ICache, 32K L1 DCache, debug and trace ; 1 MB L2 cache in CCI coherency domain,SCU(Snoop Control Unit), 128-bit ACE(AXI coherency extension) master bus interface to CCI & ACP(Accelerator coherency port) slave ; and CTM(CoreSight cross-trigger matrix), APB Multiplexer, APB ROM and APB decoder. In each of AArch32 and AArch64 execution states, there are four exception levels viz.,EL0 (unprivileged execution), EL1 (non-secure state), EL2 (virtualization - full virtualization and para virtualization) and EL3 (secure state). SCU is clocked synchronously & connects APU MPCore and ACP. The data cache is 4-way set associative and uses a physically-indexed physically-tagged (PIPT) whereas instruction cache is 2-way set associative and uses virtually-indexed physically-tagged (VIPT). The cryptography extension supports encryption and decryption, Finite field/Galois Finite fields and elliptic curve cryptography[1].

D. Cortex A8 GPU,Graphics Processing Unit

The detailed block diagram of Graphics Processing Unit(GPU) one Geometry processor(GP) is shown in Fig. 14. The detailed block diagram of Graphics Processing Unit(GPU) two Pixel processor(PP) is shown in Fig. 15.

The 64 KB L2 cache is shared by both one GP and two PPs of GPU but all of them have separate memory management units (MMU) and separate 64-bit AXI which connects to L2. At operating frequency of 400 MHz, the pixel fill rate is 800 Mpixel/sec and vertex processing rate is 40 Mvertex/sec.

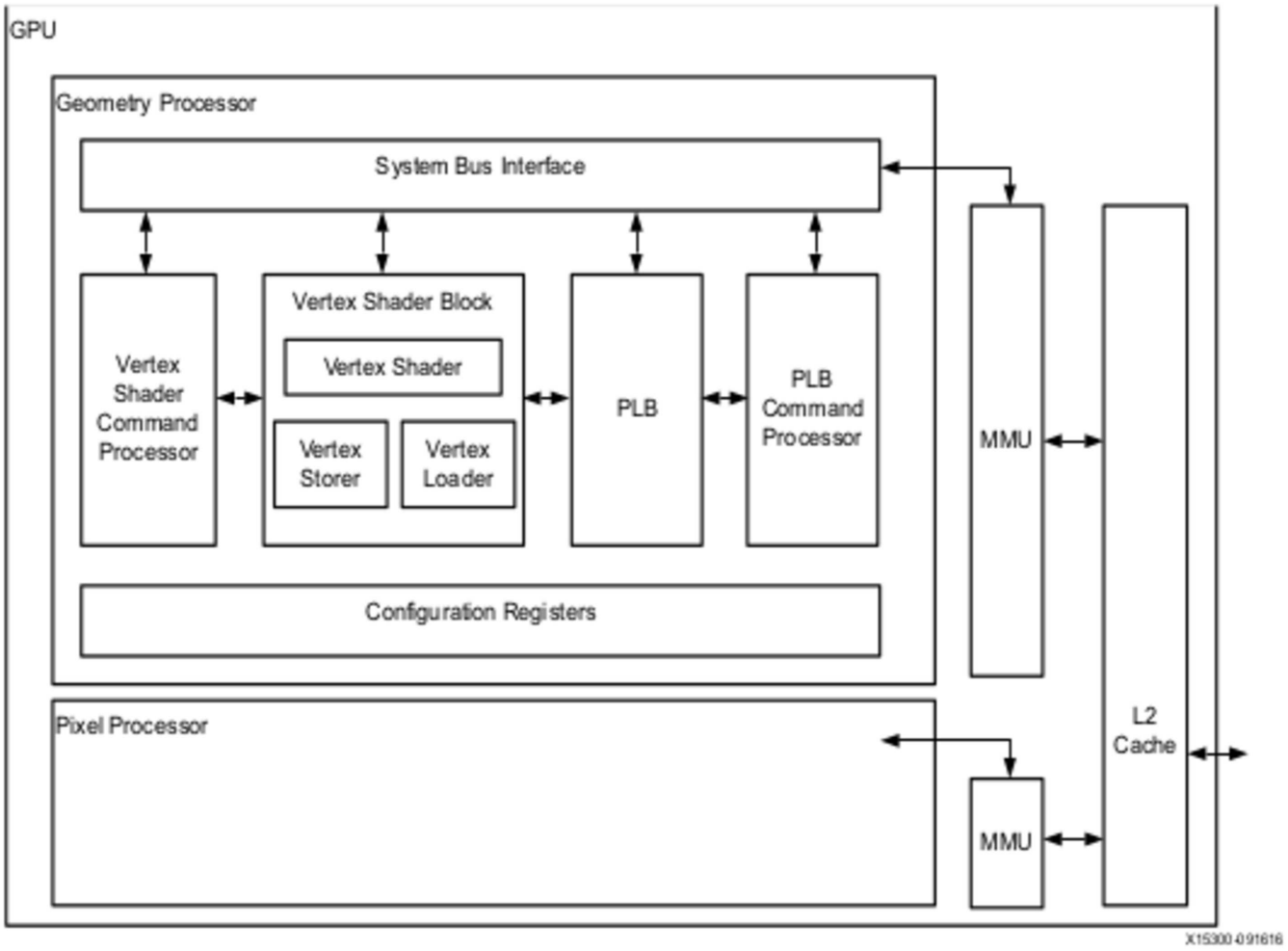

Fig. 14. Cortex A8 GPU Geometry Processor Source : AMD Xilinx

As can be seen in Fig. 14, GPU GP has vertex shader command processor, Vertex shader block(vertex shader core, vertex storer and vertex loader) and polygon list builder (PLB) with command processor which creates lists of polygons to be drawn. The vertex loader is a DMA unit which accept data from up to 16 distinct streams in floating-point formats (16-bit, 24-bit or 32-bit) or signed/unsigned fixed-point values(8-bit, 16-bit or 32-bit) or signed/unsigned normalized values (8-bit, 16-bit or 32-bit). The vertex shader core has 512 instructions for 3D transform and lighting. For QVGA or lower resolutions, PLB can create upto 300 lists as compared to allowable 512 lists.

As can be seen in Fig. 15, each of the two GPU PP consists of polygon list reader, render state words (RSWs), vertex loader, triangle setup unit, rasterizer, fragment shader, blending unit, tile buffers and title writeback unit. These read the polygon lists, render state of polygons, fetches required vertices for each primitive, compute coefficients for edge equations and varying interpolation equations, divide polygons into fragments, calculates how each fragment of a primitive looks, blends the calculated fragment, perform various tests on fragments and writes the content of tile buffer to system memory, respectively.

E. DMA & PWM

DMA is achieved from 8 channels in FPD DMA and 8 channels in LPD DMA. FPD DMA has 128-bit AXI data interface, 4 KB command buffer, non-coherent with CCI. LPD DMA has 64-bit AXI data interface, 2 KB command buffer, I/O coherent with CCI. DMA acts as an AXI-4 master. Each of the 8 channels can be programmed as secure or non-secure. Each channel is divided into two functional sides or two queues in scatter-gather DMA mode, read and write. Each linear descriptor is 128 bits and DMA channel can fetch 256 bits on every descriptor read. Each linked-list descriptor is 256 bits wide. Hybrid descriptor are achieved by chaining 128-bit linear descriptor and 256 bits linked-list descriptor.

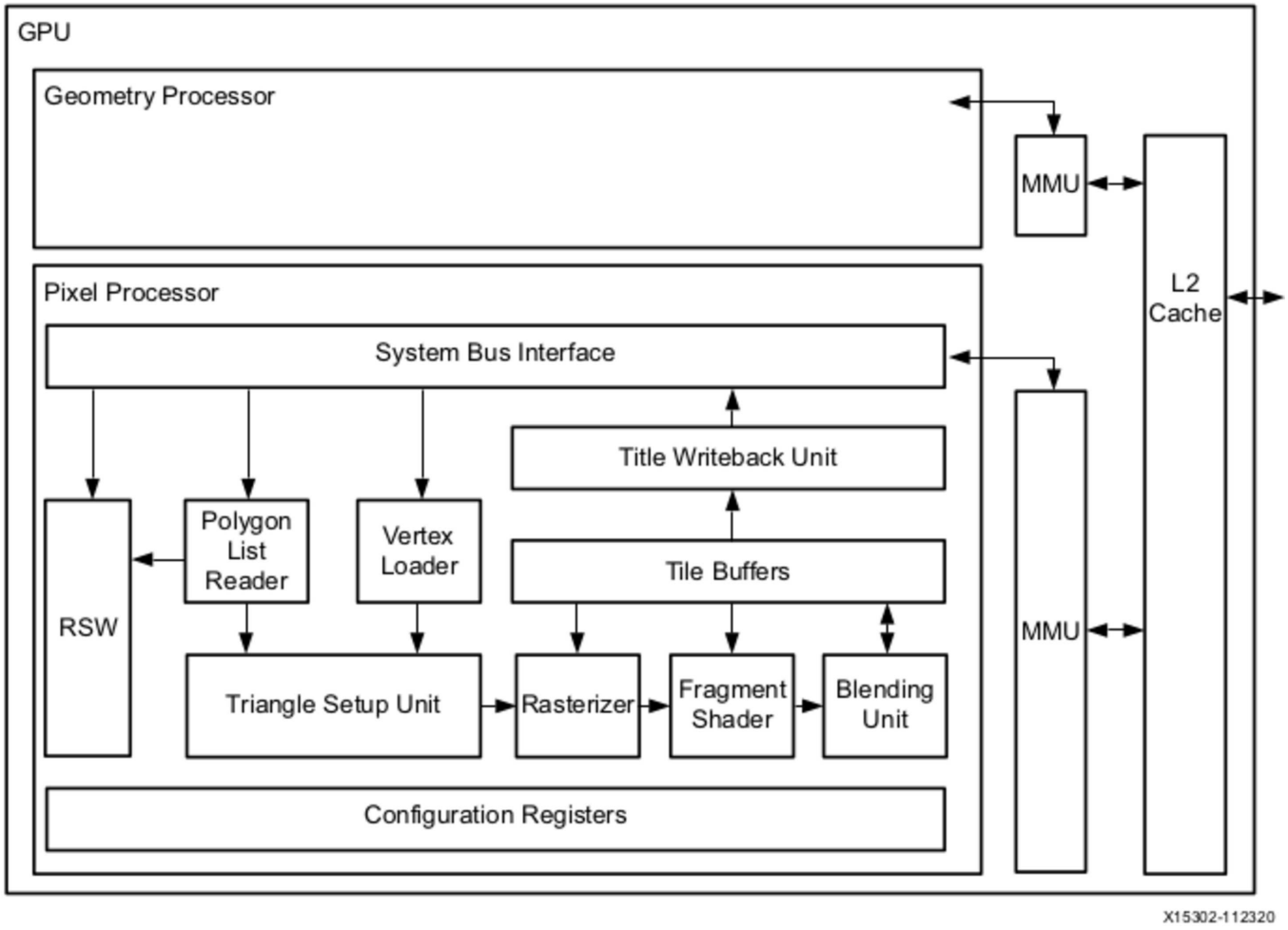

Fig. 15. Cortex A8 GPU Pixel Processor Source : AMD Xilinx

PWM can be generated from any of four triple-timer counter (TTC) units in the LPD region , where each unit comprises of three similar 32-bit timer/counters. TTC has 32-bit APB programming interface and clock can be sourced internally from PS bus clock (LPD_LSBUS_CLK) or from PL, or externally from MIO. LPD_LSBUS_CLK is 32-bit register which stores the result of LPD_LSBUS_CLK clock count during the ext_clk high or low pulse for event 1, event 2 or event 3 in Event_Register_1, Event_Register_2 and Event_Register_3. For Event_Register_1 addresses are 0x00FF110078 for TTC0, 0x00FF120078 for TTC1, 0x00FF130078 for TTC2, 0x00FF140078 for TTC3. For Event_Register_2 addresses are 0x00FF11007C for TTC0, 0x00FF12007C for TTC1, 0x00FF13007C for TTC2, 0x00FF14007C for TTC3. For Event_Register_3, addresses are 0x00FF110080 for TTC0, 0x00FF120080 for TTC1, 0x00FF130080 for TTC2, 0x00FF140080 for TTC3. Header file xtime_l.h provides access to 32-bit/64-bit TTC timer counter.

F. Clock Settings

In this subsection, various clocks which achieve gigabit-per-second levels of system performance in FPGA MPSoC is explained. To achieve this, clock management tiles has 2 phase-locked loops and segmented clock regions are arranged in tiles as compared to even other families in MPSoC, which contains 60 configurable logic blocks, 24 digital signal processor slices, 12 block RAMs, interconnect and associated clocking. In mixed-mode clock manager, number of output counters is 8 which can even drive out signal with 180° phase shift. The phase frequency detector compares both phase and frequency of the rising edges of input, PSS ref clock with frequency 33.333 MHz & feedback clock which produces an up or down signal to the charge pump and loop filter. The 8 phase taps at 45° each, giving 0°, 45°, 90°, 135°, 180°, 225°, 270°, and 315° of phase shift, and 1 variable phase tap from the voltage controlled oscillator,VCO generates integer and fractional counters. Its frequency synthesizer can provide standalone 528 MHz processor clock, 264 MHz gasket clock, 176 MHz clock, 132 MHz memory interface clock, 66 MHz

interface, and 33 MHz interface. The maximum lock time of PLL is 100 μs.

1) Automatic/Default Mode Settings: The IO-PLL(input/output phased locked loop) of Cortex R5F CPU is set with Divisor0 of 2 at 500 MHz, give actual frequency 499.994995 MHz. The RPLL (Real time procesing unit phased locked loop) of R5F CPU is set with Divisor0 of 3 at 500 MHz, give actual frequency 499.994995 MHz. The DPLL (DDR phased locked loop) of Cortex R5F CPU is set with Divisor0 of 1 at 500 MHz, give actual frequency 399.996002 MHz.

The IOPLL of UART(Universal Asynchronous Receiver/Transmitter), UART0 and UART1 and PL(Programming Logic) Fabric clock, PL Clock0, PL Clock1, PL Clock2 and PL Clock3 is set with Divisor0 of 10 and Divisor1 of 1, RPLL with Divisor0 of 15 and Divisor1 of 1 and DPLL with Divisor0 of 4 and Divisor1 of 1 at 100 MHz, give actual frequency 99.999001 MHz.

The IOPLL of System Debug clock in LPD (Low Power Domain) is set with Divisor0 of 4 and RPLL with Divisor0 of 6 at 250 MHz, give actual frequency 249.997498 MHz. The DPLL of System Debug clock in LPD (Low Power Domain) is set with Divisor0 of 5 at 500 MHz, give actual frequency 239.997604 MHz.

The IOPLL of System Debug clock in FPD (FUll Power Domain) is set with Divisor0 of 2 and APLL with Divisor0 of 6 at 250 MHz, give actual frequency 249.997498 MHz. The DPLL of System Debug clock in FPD (FUll Power Domain) is set with Divisor0 of 5 at 250 MHz, give actual frequency 239.997604 MHz.

The APLL (Application procesing unit phased locked loop) and DPLL of Cortex A8 ACPU (Application Central Processing Unit) is set with Divisor0 of 1 at 1200 MHz, give actual frequency 1199.988037 MHz. The VPLL (phased locked loop) of Cortex A8 CPU is set with Divisor0 of 1 at 1200 MHz, giving actual frequency 1066.656006 MHz. The IOPLL of Cortex A8 GPU(Graphics Processing Unit) is set with Divisor0 of 1 at 600 MHz, give actual frequency 499.994995 MHz. The DPLL of Cortex A8 GPU is set with Divisor0 of 2 at 600 MHz, give actual frequency 599.994019 MHz. The VPLL (Video phased locked loop) of Cortex A8 GPU is set with Divisor0 of 2 at 600 MHz, give actual frequency 533.328003 MHz.

The DPLL of Cortex A8 DDR (double data rate)is set with Divisor0 of 5 at 266.500 MHz, give actual frequency 239.997604 MHz. The VPLL of Cortex A8 DDR is set with Divisor0 of 4 at 266.500 MHz, give actual frequency 262.497375 MHz.

There are interconnect and switch clocks in both LPD and FPD, which have different settings.

In LPD, IOPLL of IOU Switch is set with Divisor0 of 4 and RPLL with Divisor0 of 6 at 267 MHz, give actual frequency 249.997498 MHz. In LPD, DPLL of IOU Switch is set with Divisor0 of 2 at 267 MHz, give actual frequency 199.998001 MHz.

In LPD, IOPLL of LPD_Switch is set with Divisor0 of 2 and RPLL with Divisor0 of 3 at 500 MHz, give actual frequency 499.94995 MHz. In LPD, DPLL of LPD_Switch is set with Divisor0 of 3 at 500 MHz, give actual frequency 399.996002 MHz.

In LPD, IOPLL of LSBUS and Timestamp is set with Divisor0 of 10, RPLL with Divisor0 of 15 and DPLL with Divisor0 of 4 at 100 MHz, give actual frequency 99.999001 MHz. In LPD, PSS Reference clock of timestamp is set with Divisor0 of 1 at 33.333 MHz, give actual frequency 33.333 MHz. In LPD, IOPLL and RPLL of PCAP is set with Divisor0 of 5 and DPLL with Divisor0 of 2 at 200 MHz, give actual frequency 199.998001 MHz.In LPD, IOPLL and RPLL of DMA is set with Divisor0 of 3 and DPLL with Divisor0 of 1 at 500 MHz, give actual frequency 499.994995 MHz. In LPD, IOPLL and RPLL of AMS is set with Divisor0 of 30 and Divisor1 of 1 at 50 MHz, give actual frequency 49.999500 MHz. In LPD, DPLL of AMS is set with Divisor0 of 10 and Divisor1 of 1 at 50 MHz, give actual frequency 49.999500 MHz.

In FPD, VPLL of DMA and DPDMA is set with Divisor0 of 2 at 600 MHz, give actual frequency 533.328003 MHz. In FPD, APLL and DPLL of DMA and DPDMA is set with Divisor0 of 2 at 600 MHz, give actual frequency 599.994019 MHz. In FPD, APLL and VPLL of TOPSW_MAIN is set with Divisor0 of 2 at 533.333 MHz, give actual frequency 533.328003 MHz. In FPD, DPLL of TOPSW_MAIN is set with Divisor0 of 3 at 533.333 MHz, give actual frequency 399.996002 MHz.

In FPD, APLL and DPLL of TOPSW_LSBUS is set with Divisor0 of 12 and IOPL with Divisor0 of 5 at 100 MHz, give actual frequency 99.999001 MHz.

2) Manual Mode Settings: In manual mode, fractional multipliers in increments of 1/8th (0.125) viz. 0.2871 for VPLL or 0.779 for RPLL etc. can be multiplied with intergers of source clocks and divisors can be changed as needed, provided PLL is set to operate in a specific frequency range.

Thus,

If fractional divide is 0.125, then static phase shift step is $360/(0.125 \times 8)^{\circ} = 360^{\circ}$.

If fractional divide is 0.2871, then static phase shift step is $360/(0.2871 \times 8)^{\circ} = 156.739811912^{\circ}$.

If fractional divide is 0.779, then static phase shift step is $360/(0.779 \times 8)^{\circ}$ = 57.766367137°.

If VCO runs at 33 MHZ, then phase resolution is $1/(56 \times 33\ MHz)$ is 541.12554 pico seconds.

If VCO runs at 100 MHZ, then phase resolution is $1/(56 \times 100\ MHz)$ is 178.57143 pico seconds.

If VCO runs at 400 MHZ, then phase resolution is $1/(56 \times 400\ MHz)$ is 44.64286 pico seconds.

If VCO runs at 600 MHZ, then phase resolution is $1/(56 \times 600\ MHz)$ is 29.7619 pico seconds.

If VCO runs at 1 GHZ, then phase resolution is $1/(56 \times 1\ GHz)$ is 17.85714 pico seconds.

If VCO runs at 1.6 GHZ, then phase resolution is $1/(56 \times 1.6\ GHz)$ is 11.16071 pico seconds.

Conclusion And Futue Work

The author has used datasheets, reference manual and minor calculations in drawing various contrasts in power supply, current consumption, PWM, and DMA. As these processors are in physical procession with author, the results are used in author's personal R& D and projects.

There can be more additions with details but what gives the comparison is brought to light.

Competing Interests

The author declares no competing interest. This manuscript has not been accepted or published by any journal.

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Disclosure statement

The author declares no potential conflict of interest.

References

References are known and elementary for any school student or graduate, degree holder.

Pls refer datasheet, reference manual.

References

[1] Bansal, Abhishek (2023). Implementing Elliptic Curve & HyperElliptic Curve Cryptography on Crypto Hardware Accelerator of MPSoC. TechRxiv. Preprint. https://doi.org/10.36227/techrxiv.21778709

[2] click : Path Programmable III .

Abhishek Bansal His International and Legal profile can be seen at ORCiD with identification number 0000-0002-2572-9004 or click here.